DG508A/509A

Single 8-Ch/Differential 4-Ch CMOS Analog Multiplexers

Features

- Low On-Resistance: 240 Ω
- TTL and CMOS Logic Compatible
- Low Power: 30 mW
- Break-Before-Make Switching
- 44-V Power Supply Rating
- Transition Time: 600 ns

Benefits

- Easily Interfaced
- Low Power Consumption
- Low System Crosstalk
- Wide Analog Signal Range

Applications

- Communication Systems
- ATE
- Data Acquisition Systems
- Audio Signal Routing and Multiplexing
- Medical Instrumentation

Description

The DG508A, an 8-channel single-ended analog multiplexer, is designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2).

The DG509A, a dual 4-channel analog multiplexer, is designed to connect one of four differential inputs to a common output as determined by its 2-bit binary address (A_0, A_1) logic. Break-before-make switching action protects against momentary shorting of the input signals.

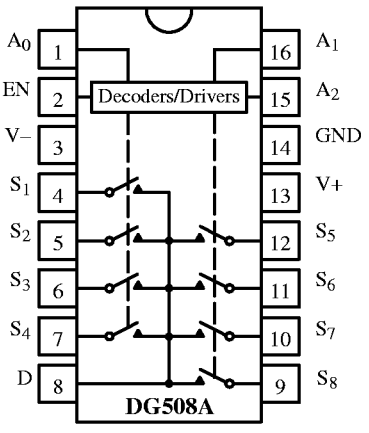
A channel in the on state conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails, normally 30 V peak-to-peak. An enable (EN) function allows for device selection when several multiplexers are used All control inputs, address (A_X) and enable (EN) are TTL or CMOS compatible over the full specified operating temperature range.

Fabricated in the Siliconix Plus-40 process, the absolute maximum voltage rating is extended to 44 V, allowing increased operating headroom for standard ± 15-V signal swings and operation with ± 20-V supplies. An epitaxial layer prevents latch up.

For applications requiring address data latching, the DG528/529 is recommended. DG408/409 is recommended for higher precision applications. For wideband/video routing and multiplexing, the DG538A is recommended.

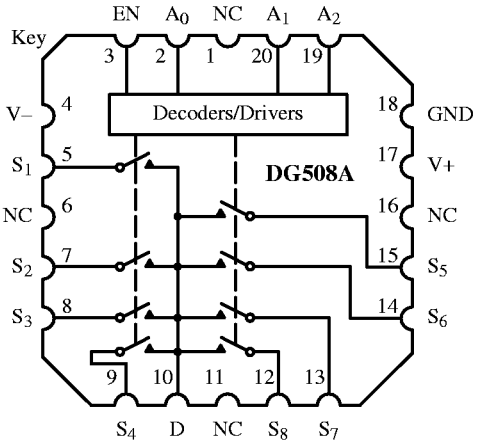
Functional Block Diagrams and Pin Configurations

Dual-In-Line and SOIC



Top View

LCC



Top View

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70067.

Functional Block Diagrams and Pin Configurations (Cont'd)

Ordering Information – DG508A

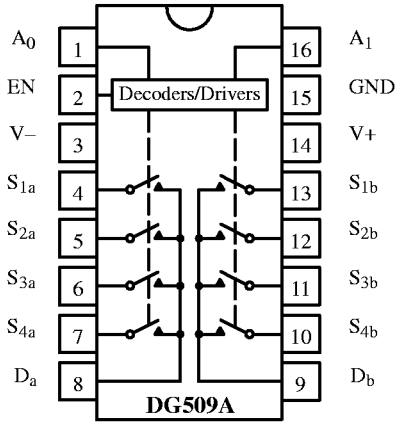
Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG508ACJ
–25 to 85°C	16-Pin CerDIP	DG508ABK
–40 to 85°C	16-Pin Narrow SOIC	DG508ADY
–55 to 125°C	16-Pin CerDIP	DG508AAK
		DG508AAK/883
	LCC-20	DG508AAZ/883
	16-Pin Sidebraze	7705201EA
		7705201EC
	16-Pin Flat Pack	7705201FA
		7705201FC
	16-Pin Sidebraze	JM38510/19007BEA
		JM38510/19007BEC

Truth Table — DG508A

A_2	A_1	A_0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

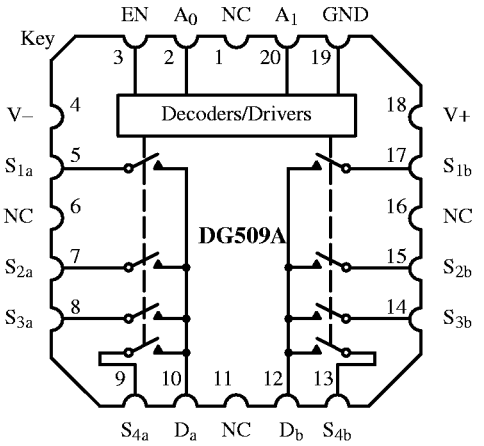
Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

Dual-In-Line and SOIC



Top View

LCC



Top View

Ordering Information – DG509A

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG509ACJ
–25 to 85°C	16-Pin CerDIP	DG509ABK
–40 to 85°C	16-Pin Narrow SOIC	DG509ADY
–55 to 125°C	16-Pin CerDIP	DG509AAK
		DG509AAK/883
	LCC-20	DG509AAZ/883
	16-Pin Sidebraze	JM38510/19008BEA
		JM38510/19008BEC

Truth Table — DG509A

A_1	A_0	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

Absolute Maximum Ratings

Voltage Referenced to V–
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[a], V_S, V_D ..... (V–) –2 V to (V+) +2 V or 20 mA, whichever occurs first
Current (Any Terminal, Except S or D) ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA
Storage Temperature (K Suffix) ..... –65 to 150°C
(J and Y Suffix) ..... –65 to 125°C

Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] ..... 470 mW
16-Pin Narrow SOIC[c] ..... 600 mW
16-Pin CerDIP[d] ..... 900 mW
LCC-20[d] ..... 900 mW

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 6.3 mW/°C above 75°C.
d. Derate 12 mW/°C above 75°C.

Specifications[a]

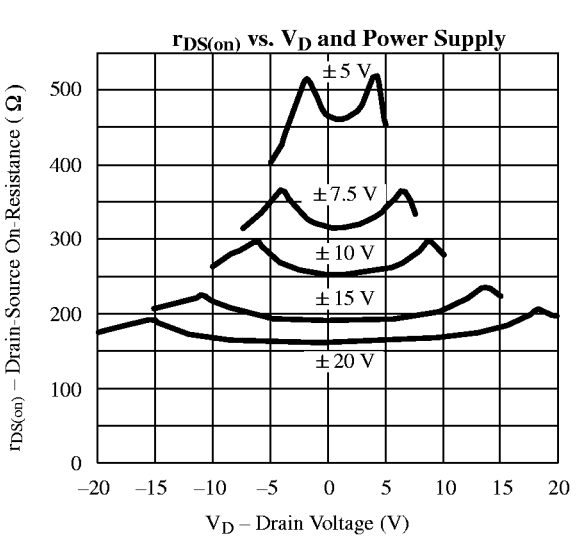
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V, V_{IN} = 2.4 V, 0.8 V[f]		Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	D Suffix –40 to 85°C Min[d]	D Suffix –40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		–15	15	–15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ± 10 V, I_S = –200 µA		Room Full	240		400 500		450 550	Ω
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$	–10 V < V_S < 10 V		Room	6					%
Source Off Leakage Current	$I_{S(off)}$	V_{EN} = 0 V, V_S = ± 10 V V_D = ∓ 10 V		Room Full		–1 –50	1 50	–5 –50	5 50	nA
Drain Off Leakage Current	$I_{D(off)}$	V_{EN} = 0 V V_D = ± 10 V V_S = ∓ 10 V	DG508A	Room Full		–10 –200	10 200	–20 –200	20 200	
			DG509A	Room Full		–10 –100	10 100	–20 –100	20 100	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ± 10 V	DG508A	Room Full		–10 –200	10 200	–20 –200	20 200	
			DG509A	Room Full		–10 –100	10 100	–20 –100	20 100	
Digital Control										
Logic Input Current Input Voltage High	I_{AH}	V_A = 2.4 V		Room Full	–0.002	–10 –30		–10 –30		µA
		V_A = 15 V		Room Full	0.006		10 30		10 30	
Logic Input Current Input Voltage Low	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Room Full	–0.002	–10 –30		–10 –30		
Dynamic Characteristics										
Transition Time	t_{TRANS}	See Figure 2		Room	0.6		1			µs
Break-Before-Make Time	t_{OPEN}	See Figure 4		Room	0.2					
Enable Turn-On Time	$t_{ON(EN)}$	See Figure 3		Room	1		1.5			
Enable Turn-Off Time	$t_{OFF(EN)}$			Room	0.4		1.0			
Charge Injection	Q	See Figure 5		Room	6					pC
Off Isolation	OIRR	V_{EN} = 0 V, R_L = 1 kΩ, C_L = 15 pF V_S = 7 V_{RMS}, f = 500 kHz		Room	68					dB
Logic Input Capacitance	C_{in}	f = 1 MHz		Room	8					pF
Source Off Capacitance	$C_{S(off)}$	V_{EN} = 0 V, V_S = 0 V, f = 140 kHz		Room	6					
Drain Off Capacitance	$C_{D(off)}$	V_{EN} = 0 V, V_D = 0 V f = 140 kHz	DG508A	Room	25					
			DG509A	Room	12					

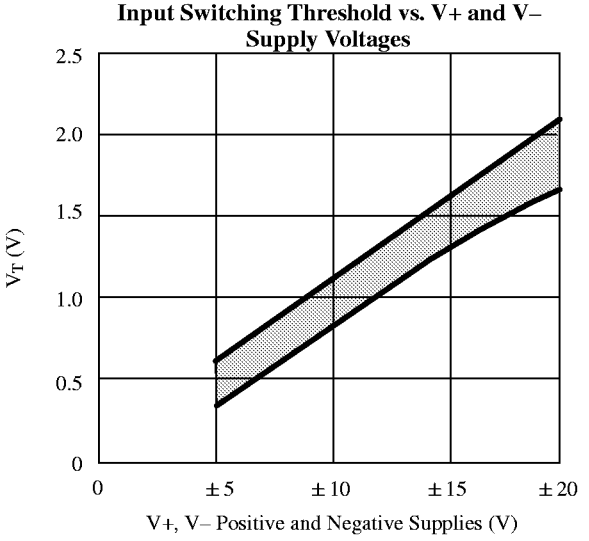
Specifications[a] (Cont'd)

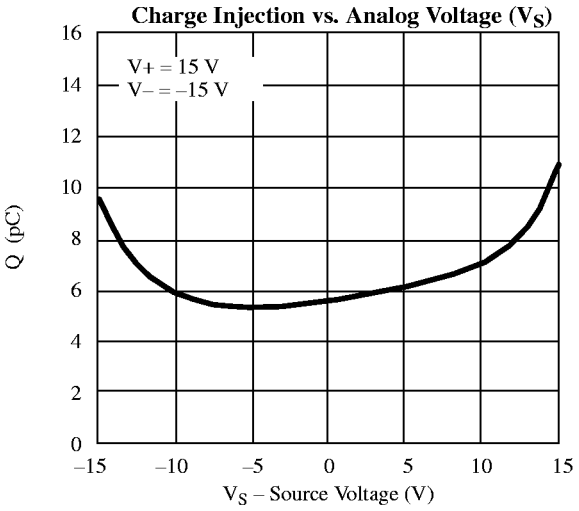
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	D Suffix –40 to 85°C Min[d]	D Suffix –40 to 85°C Max[d]	Unit
Power Supplies									
Positive Supply Current	I+	V_{EN} = 0 V or 2.4 V	Room	1.3		2.4		2.4	mA
Negative Supply Current	I–		Room	–0.7	–1.5		–1.5		

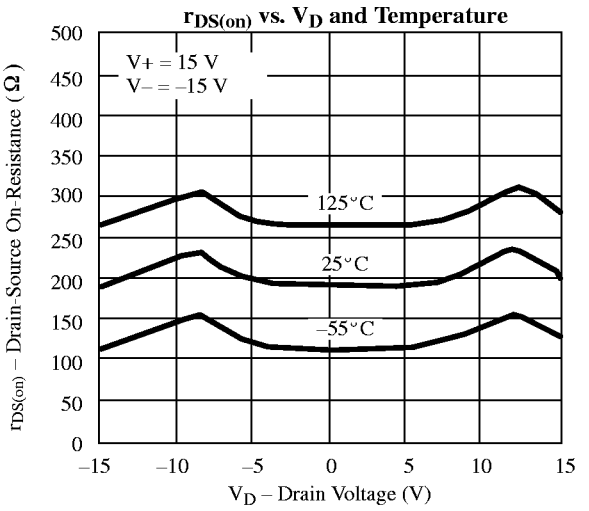
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics



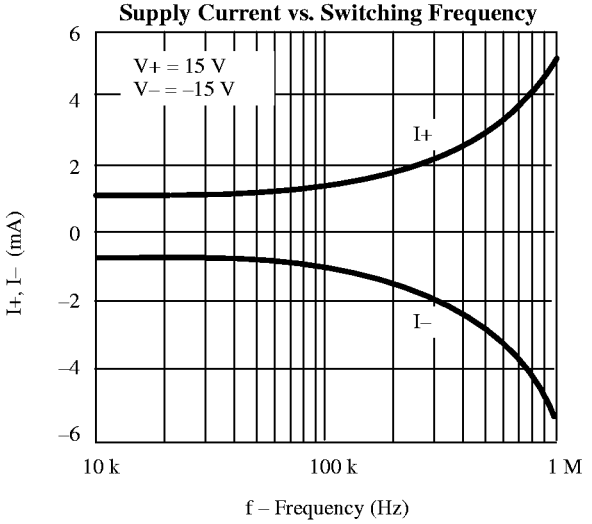




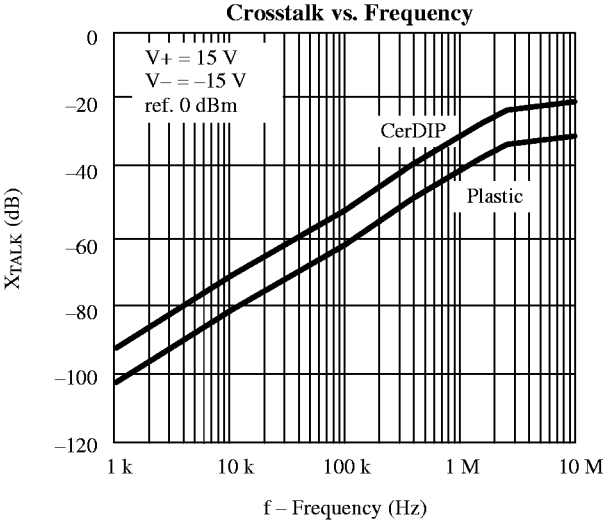


Typical Characteristics (Cont'd)

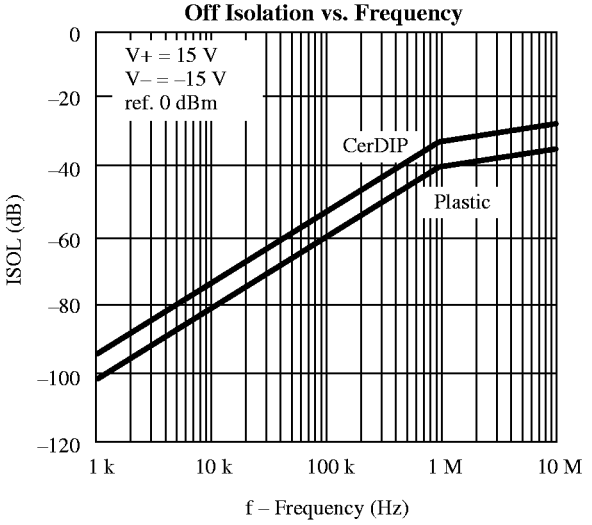
Supply Current vs. Switching Frequency



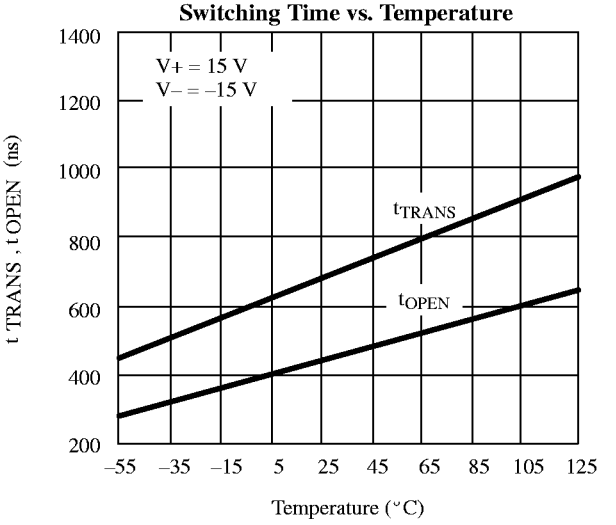
Crosstalk vs. Frequency



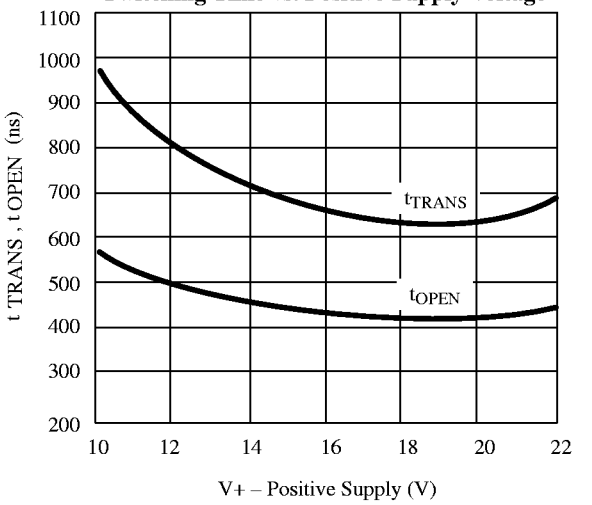
Off Isolation vs. Frequency



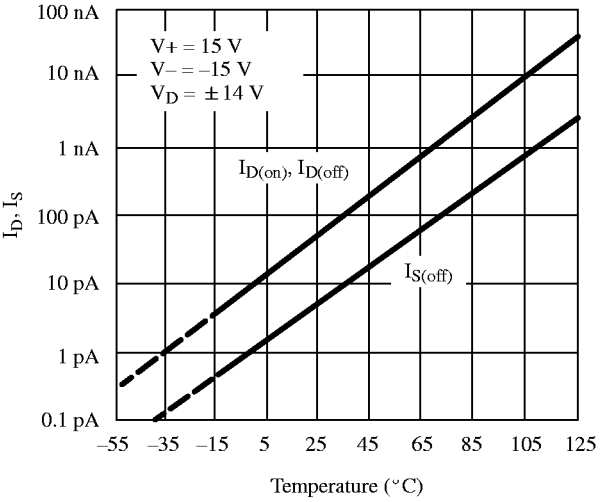
Switching Time vs. Temperature



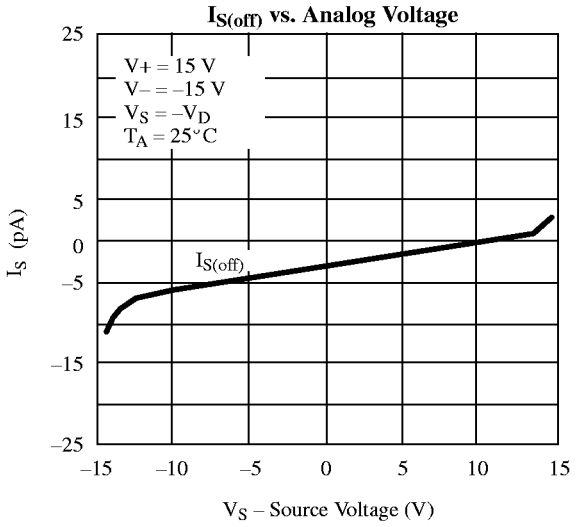
Switching Time vs. Positive Supply Voltage

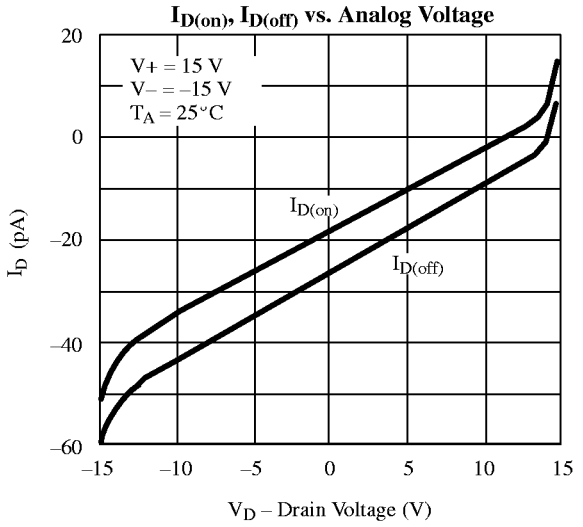


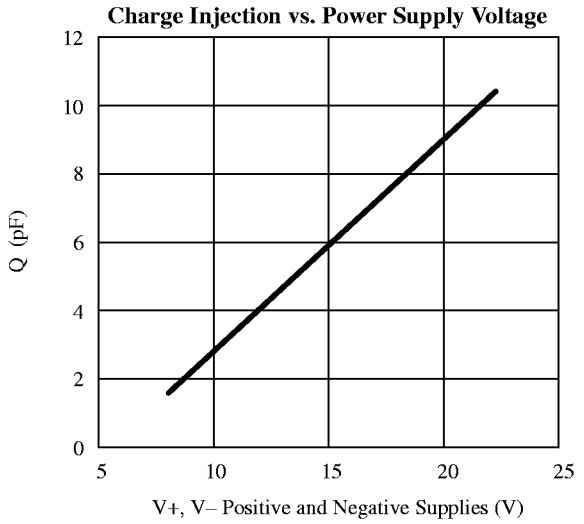
Leakages vs. Temperature



Typical Characteristics (Cont'd)







Schematic Diagram (Typical Channel)

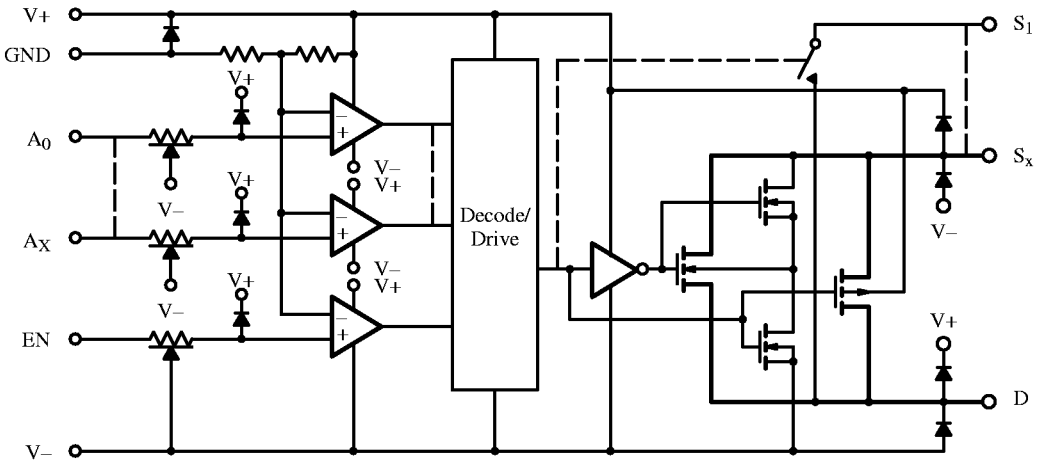


Figure 1.

Test Circuits

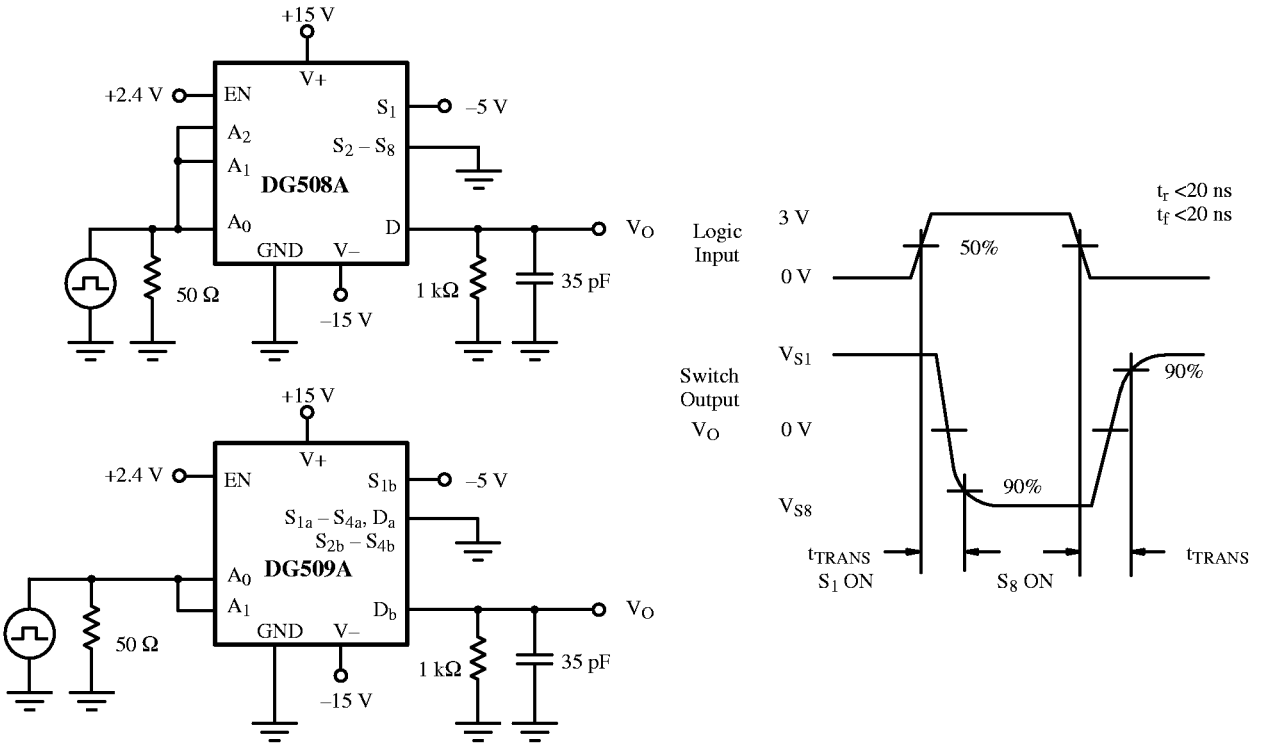


Figure 2. Transition Time

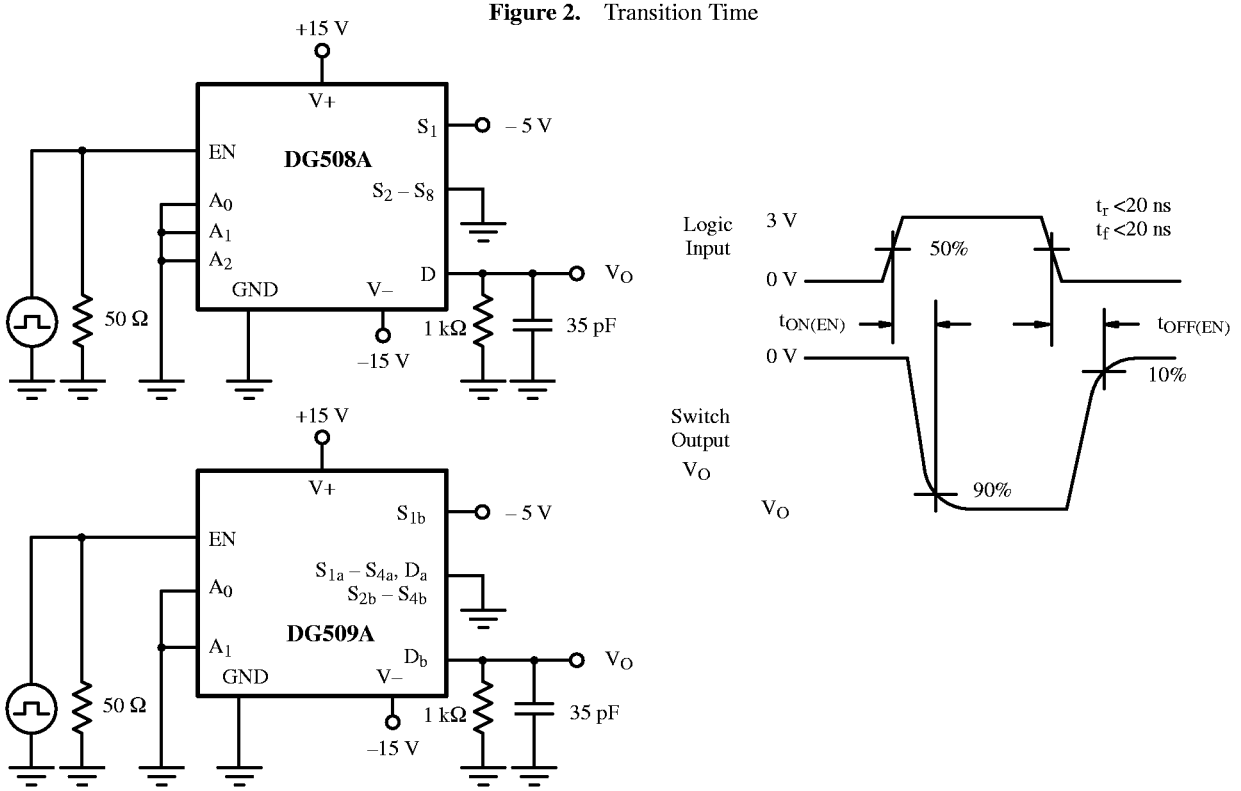


Figure 3. Enable Switching Time

Test Circuits (Cont'd)

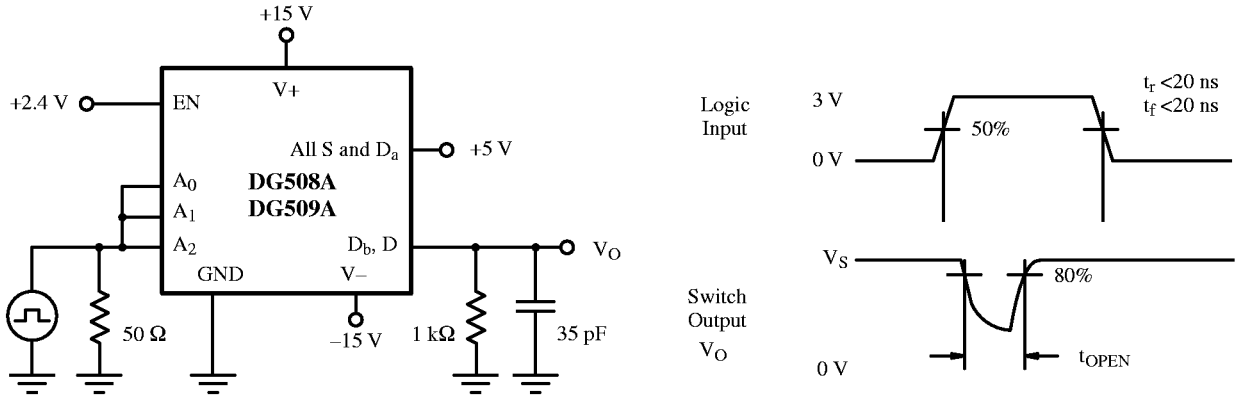


Figure 4. Break-Before-Make Interval

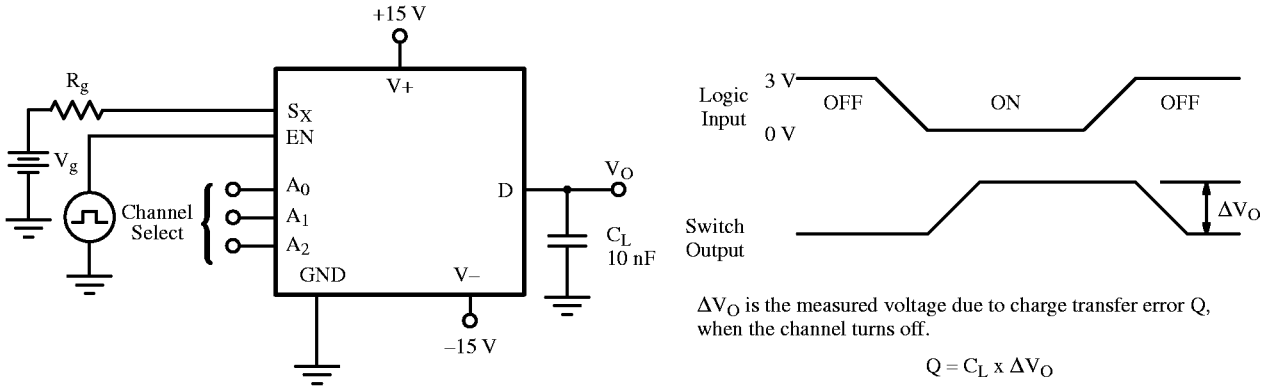


Figure 5. Charge Injection

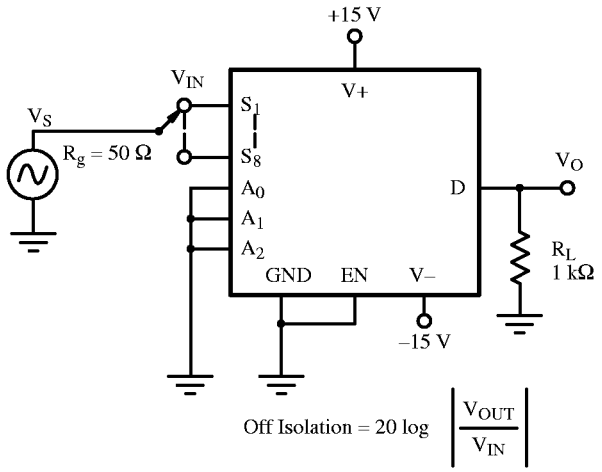


Figure 6. Off Isolation

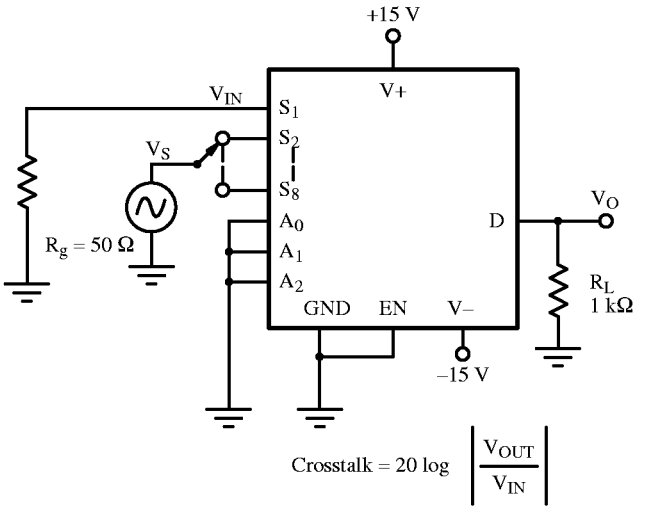


Figure 7. Crosstalk

Test Circuits (Cont'd)

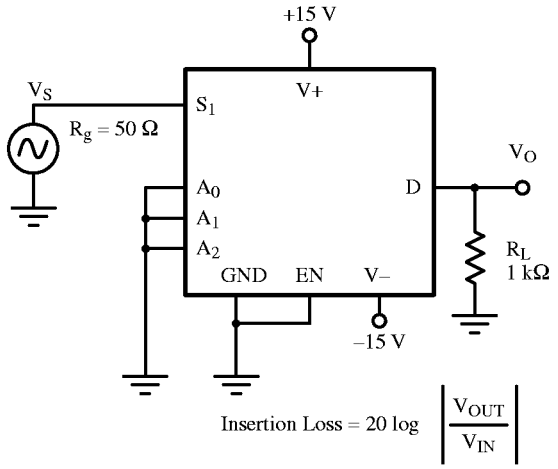


Figure 8. Insertion Loss

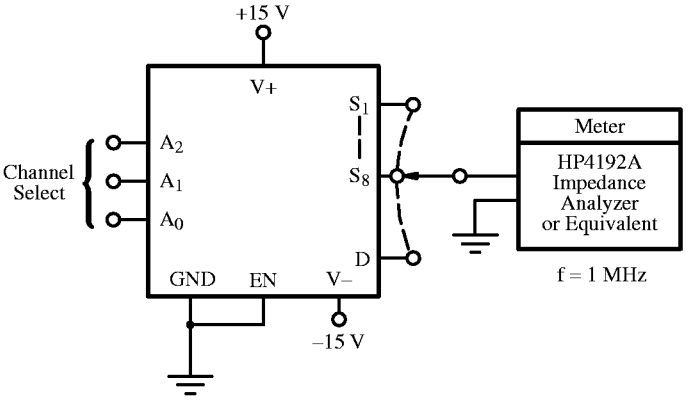


Figure 9. Source Drain Capacitance

Applications[a]

V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
15	–15	2.4/0.8	–15 to 15
10	–12	2.4/0.8	–12 to 12
12	–10	2.4/0.6	–10 to 10
8[b]	–8	2.4/0.4	–8 to 8

Notes:
a. Application hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
b. Operation below ±8 V is not recommended.

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 11). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V– value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference between V_S and the V– rail doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V–, but it preserves the low channel resistance and low leakage characteristics.

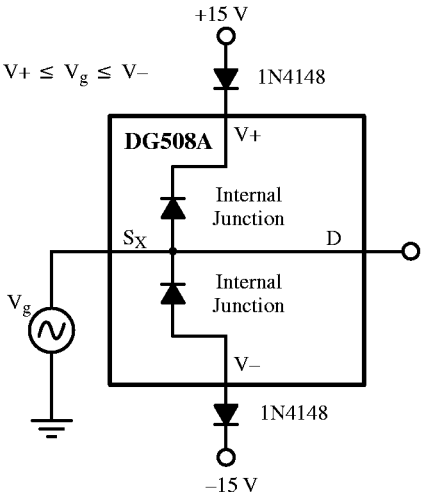


Figure 10. Overvoltage Protection Using Blocking Diodes

Overvoltage Protection (Cont'd)

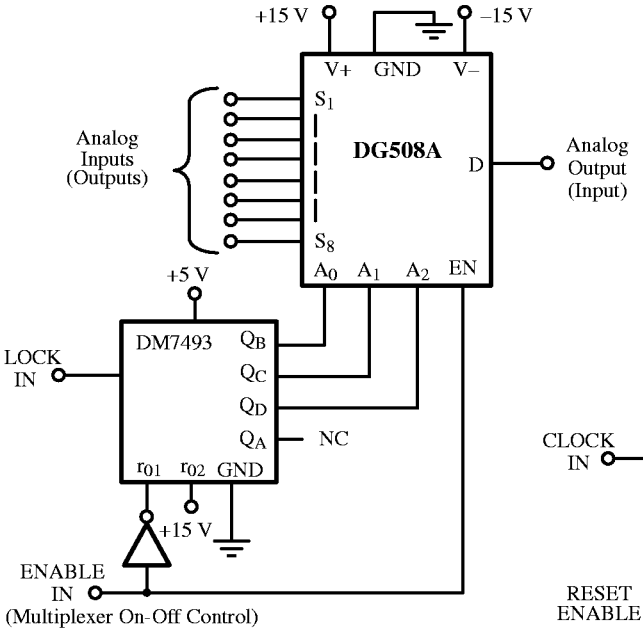


Figure 11. 8-Channel Sequential Multiplexer/ Demultiplexer

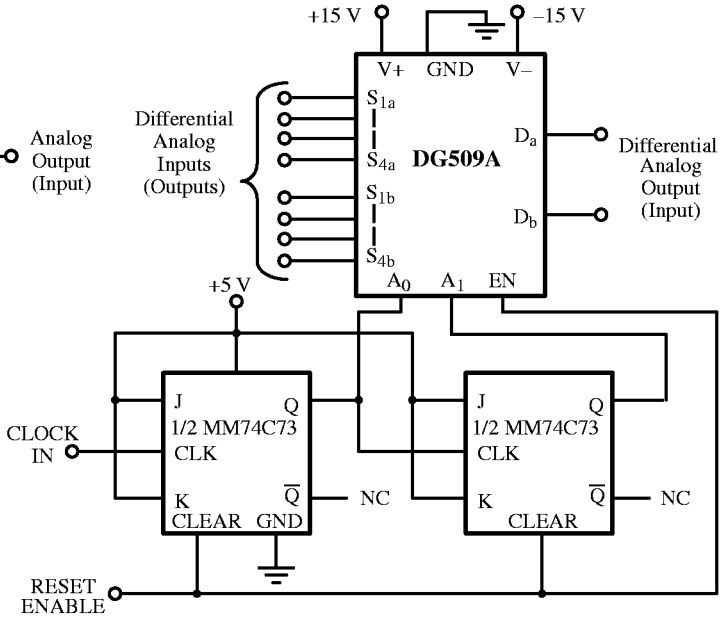
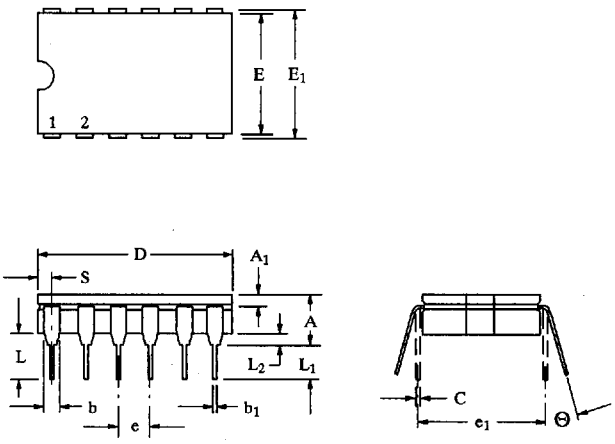


Figure 12. Differential 4-Channel Sequential Multiplexer/ Demultiplexer

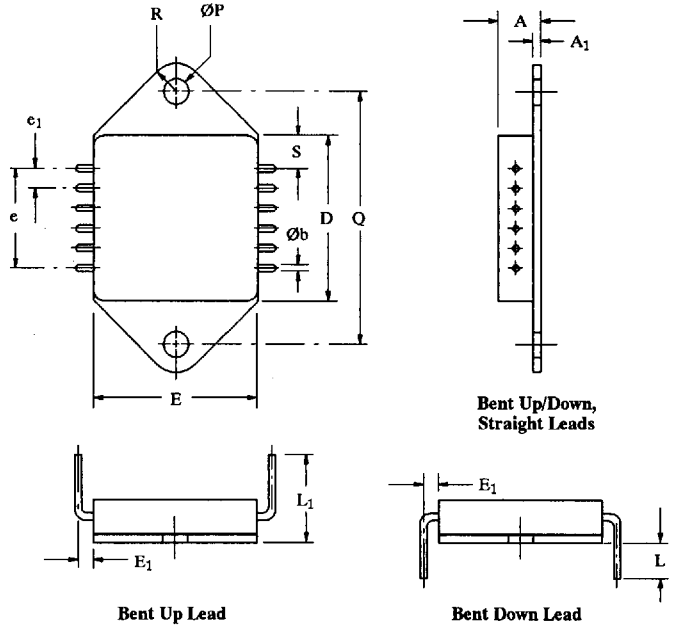
Package Information

■ Ceramic DIP, 8- to 16-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A_1	1.27	2.16	0.050	0.085
b	1.14	1.65	0.045	0.065
b_1	0.38	0.51	0.015	0.020
C	0.20	0.30	0.008	0.012
D–8	9.40	10.16	0.370	0.400
D–14	19.05	19.56	0.750	0.770
D–16	19.05	19.56	0.750	0.770
E	6.60	7.62	0.260	0.300
E_1	7.62	8.26	0.300	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L_1	3.18	3.81	0.125	0.150
L_2	0.51	1.14	0.020	0.045
S–8	0.64	1.52	0.025	0.060
S–14	1.65	2.41	0.065	0.095
S–16	0.38	1.14	0.015	0.045
Θ	0°	15°	0°	15°

■ Hermetic Power Module



Bent Up/Down, Straight Leads

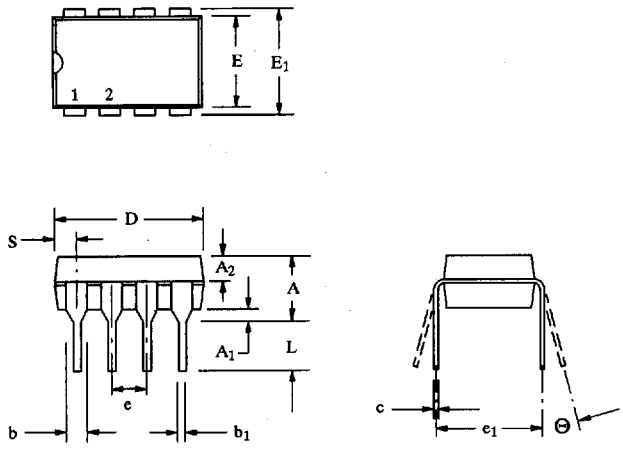
Bent Up Lead

Bent Down Lead

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	6.10	7.11	0.240	0.280
A_1	1.14	1.40	0.045	0.055
Øb	0.89	1.14	0.035	0.045
D	24.89	25.91	0.980	1.020
E	24.89	25.91	0.980	1.020
E_1	2.79	3.30	0.110	0.130
e	15.62	16.13	0.615	0.635
e_1	2.92	3.43	0.115	0.135
L	4.44	6.35	0.175	0.250
L_1	12.32	–	0.485	–
ØP	3.84	4.09	0.151	0.161
Q	38.35	38.86	1.510	0.161
R	4.19	4.44	0.165	0.175
S	4.57	4.95	0.180	0.195

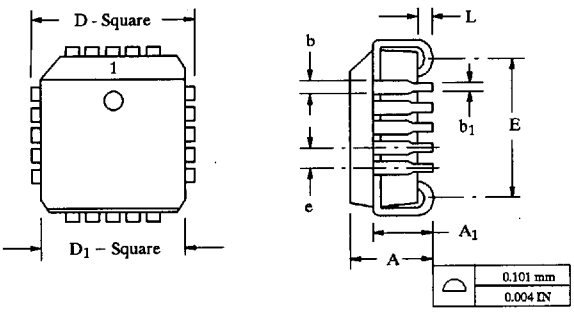
Package Information

■ Plastic DIP, 8- to 20-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D–8	9.65	11.68	0.380	0.460
D–14	17.27	19.30	0.680	0.760
D–16	18.93	21.33	0.745	0.840
D–20	24.89	26.92	0.980	1.060
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S–8	1.02	2.03	0.040	0.080
S–14	1.02	2.03	0.040	0.080
S–16	0.38	1.52	0.015	0.060
S–20	1.02	2.03	0.040	0.080
Θ	0°	15°	0°	15°

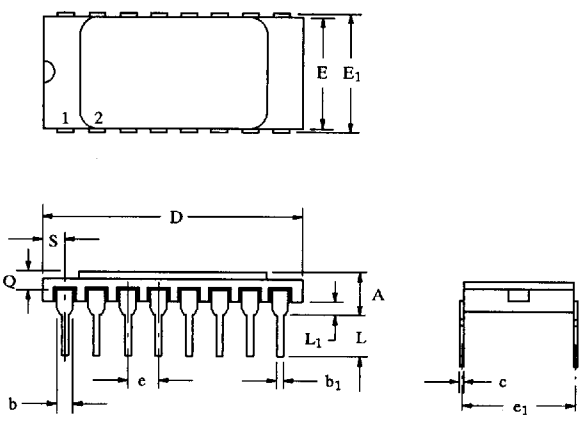
■ PLCC Package, 20-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.20	4.57	0.165	0.180
A_1	2.29	3.04	0.090	0.120
b	0.66	0.81	0.026	0.032
b_1	0.33	0.55	0.013	0.021
D	9.78	10.03	0.385	0.395
D_1	8.89	9.04	0.350	0.356
E	7.37	8.38	0.290	0.330
e	1.27 BSC		0.050 BSC	
L	0.51	–	0.020	–

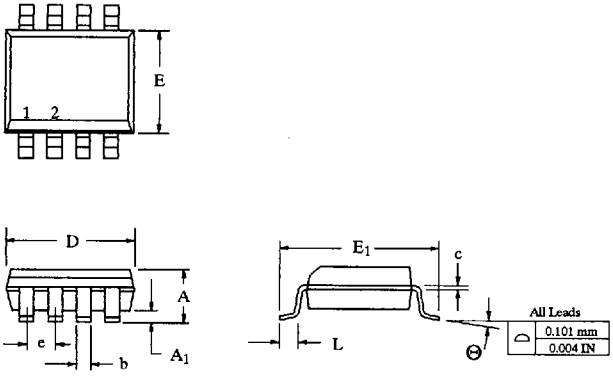
Package Information

■ Sidebraze DIP, 14- to 24-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	2.67	4.44	0.105	0.175
b	0.97	1.52	0.038	0.060
b_1	0.38	0.53	0.015	0.021
c	0.20	0.30	0.008	0.012
D–14	17.53	19.55	0.690	0.770
D–16	19.56	21.08	0.770	0.830
D–20	24.89	26.16	0.890	1.030
D–24	29.97	31.24	1.180	1.230
E	7.12	7.87	0.280	0.310
E_1	7.37	8.25	0.290	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.18	4.44	0.125	0.175
L_1	0.64	1.39	0.025	0.055
Q	0.25	–	0.010	–
S–14	0.77	2.41	0.030	0.095
S–16	0.51	1.65	0.020	0.065
S–20	0.77	1.65	0.030	0.065
S–24	0.77	2.41	0.030	0.095

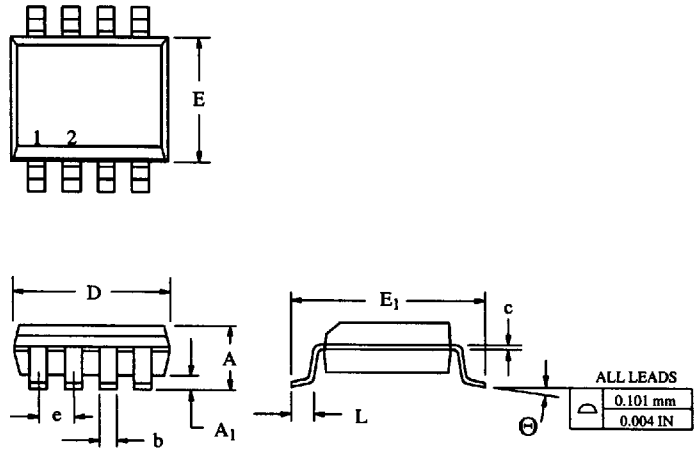
■ SO Package, 8- to 16-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.45	0.014	0.018
c	0.18	0.23	0.007	0.009
D-8	4.69	5.00	0.185	0.196
D-14	8.55	8.75	0.336	0.344
D-16	9.80	10.00	0.385	0.393
E	3.50	4.05	0.140	0.160
E_1	5.70	6.30	0.224	0.248
e	1.27 BSC		0.050 BSC	
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°

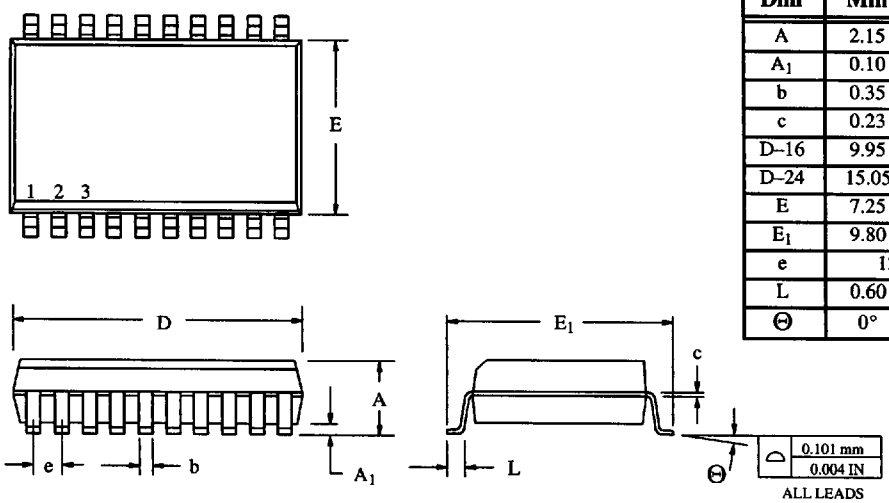
L	0.13	0.25	0.005	0.010
S	0.44	0.55	0.017	0.022
Θ	0°	8°	0°	8°

SOIC, 8–16 Leads



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.45	0.014	0.018
c	0.18	0.23	0.007	0.009
D-8	4.69	5.00	0.185	0.196
D-14	8.55	8.75	0.336	0.344
D-16	9.80	10.00	0.385	0.393
E	3.50	4.05	0.140	0.160
E_1	5.70	6.30	0.224	0.248
e	1.27 BSC		0.050 BSC	
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°

SOIC Wide-Body, 16–24 Leads



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	2.15	2.90	0.085	0.114
A_1	0.10	0.30	0.004	0.012
b	0.35	0.45	0.014	0.018
c	0.23	0.28	0.009	0.011
D–16	9.95	10.75	0.392	0.423
D–24	15.05	15.85	0.593	0.624
E	7.25	8.00	0.285	0.315
E_1	9.80	10.60	0.386	0.417
e	127 BSC		0.050 BSC	
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°