TRIPLE OPERATIONAL AMPLIFIER

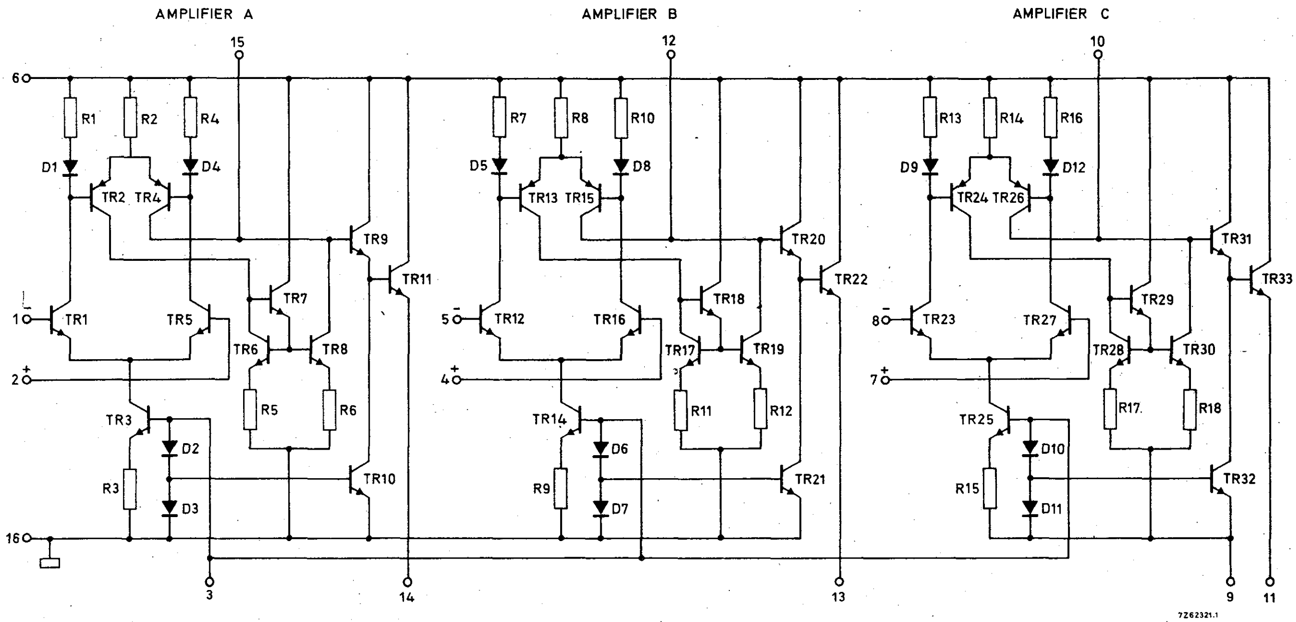
The TCA220 is a monolithic integrated circuit, consisting of three identical high-gain amplifiers.
The amplifiers have a differential input stage and an emitter-follower output stage, which can supply a current up to 100 mA.
The unity-gain frequency with 6 dB/octave compensation is 5 MHz minimum. No latch-up occurs if the input voltage range is exceeded.

QUICK REFERENCE DATA

Positive supply voltage	V_P	nom.	6	V
Negative supply voltage	V_N	nom.	6	V
Voltage gain	G_v	typ.	4000	
Common mode rejection ratio	CMRR	typ.	90	dB
Supply voltage rejection ratio	SVRR	typ.	200	μV/V
Input offset voltage	V_{io}	typ.	2	mV
Input offset current	I_{io}	typ.	0,2	μA

PACKAGE OUTLINE plastic 16-lead dual in-line (see general section).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

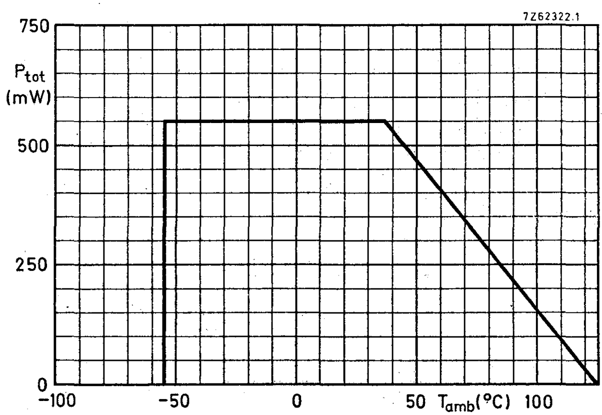
Voltages

Supply voltage	V_{6-16}	max.	18	V
Common mode input voltage	V_i	max.	18	V 1)
Differential input voltages	$\pm V_{1-2}$; $\pm V_{5-4}$; $\pm V_{8-7}$	max.	5,0	V
Pin No. 9 voltage	V_{9-16}	max.	0	V 2)

Currents

Input currents (pins, 1, 2, 4, 5, 7, 8)	I_1; I_2; I_4; I_5; I_7; I_8	max.	0,5	mA
Output currents (pins 14, 13, 11)	$-I_{14}$; $-I_{13}$; $-I_{11}$	max.	100	mA
Bias current (pin 3)	I_3	max.	5,0	mA

Total power dissipation



Temperatures

Storage temperature	T_{stg}	−55 to +125		°C
Junction temperature	T_j	max.	125	°C

1) For a total supply voltage less than 18 V, the absolute maximum input voltage is equal to the supply voltage.

2) If amplifier C is used, pin 9 must be connected to pin 16.

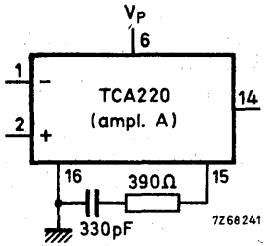
THERMAL RESISTANCE

From junction to ambient	R_{th}	max.	160	°C/W

CHARACTERISTICS (each amplifier) at V_P = 6 V; $-V_N$ = 6 V; T_{amb} = 25 °C
R_L = 10 kΩ (unless otherwise specified)

Voltage gain at ± V_{OM} = 3,5 V	G_v	typ.	4000	
Input offset voltage at $R_S \leq$ 200 Ω	V_{io}	typ.	2	mV
		<	10	mV
Input bias current	I_i	typ.	1,0	μA
		<	2,0	μA
Input offset current	I_{io}	typ.	0,2	μA
Common mode rejection ratio at R_S = 2 kΩ	CMRR	typ.	90	dB
Input voltage range	V_i		−4,3 to +5,6	V
Differential input resistance	R_i	>	25	kΩ
Supply voltage rejection ratio at R_S = 2 kΩ	SVRR	typ.	200	μV/V
Peak output voltage swing	V_{OM}		−6 to +3,5	V
Total current at V_o = 0; R_L = 10 kΩ	I_{tot}	typ.	1,0	mA
at V_o = 0; R_L = ∞	I_{tot}	typ.	0,4	mA
Slew rate (unity-gain)		typ.	0,4	V/μs
Bias current (all three amplifiers together)	I_3	>	200	μA[1]
Channel separation between amplifiers A and B		typ.	94	dB[2]
between amplifiers A and C		typ.	130	dB[2]
between amplifiers B and C		typ.	110	dB[2]

Frequency compensation circuit



[1] The voltage at pin 3 is always 2 diode voltages (approx. 1,5 V) above the negative supply voltage; if the bias current in obtained from the positive supply voltage a dropping resistor $R_P \leq \frac{V_P - V_N - 1,5}{200 \cdot 10^{-6}}$ gives minimum power consumption.

[2] Channel separation defined as 20 log $\frac{V_{oA}}{V_{oB}}$ x G_B, if G_B is the closed loop gain of amplifier B.