BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1032H

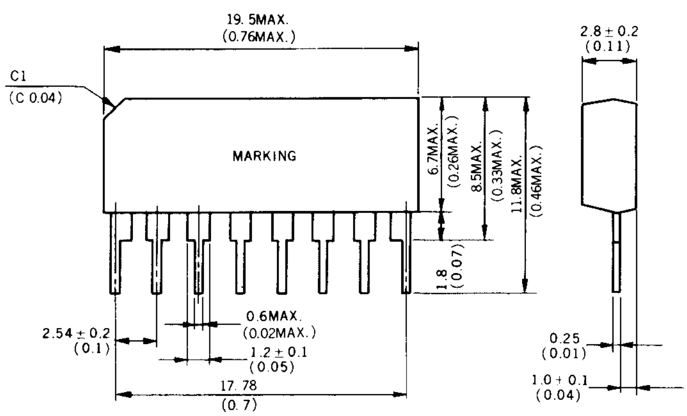
DUAL LOW NOISE PREAMPLIFIER
SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

DESCRIPTION

The μPC1032H is a silicon monolithic integrated circuit designed for use as a 2 channel preamplifier for a car stereo set. The device has features of low noise, high gain, high output voltage and wide supply voltage range.
Especially, as an advanced production process is used, the device has an excellent feature of very low pulsive noise.
An internal voltage regulator circuit permits the μPC1032H to operate satisfactorily over wide variation of supply voltage.

PACKAGE DIMENSIONS

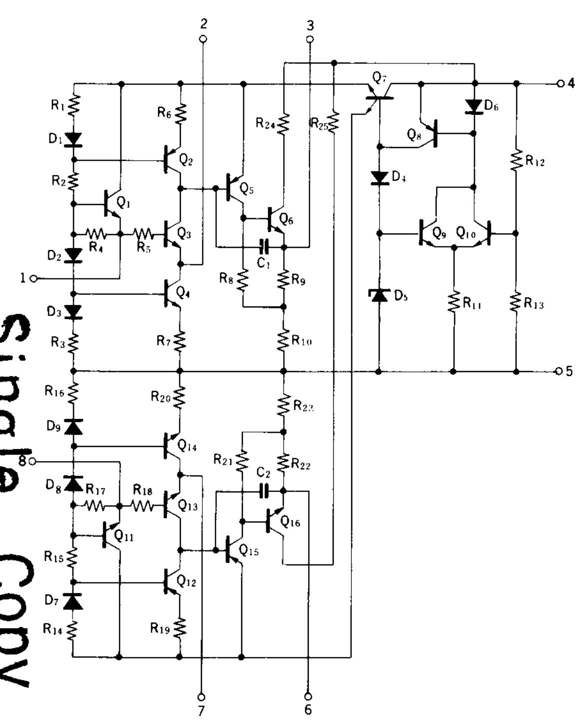
in millimeters (inches)



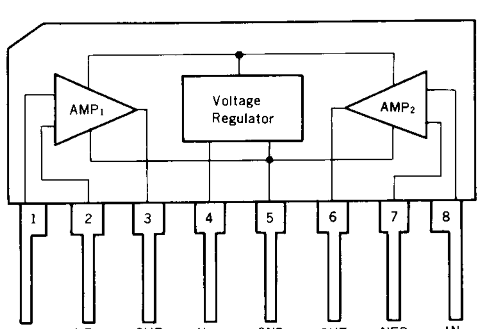
FEATURES

- Two channel
- Wide supply voltage range
- Minimum number of external parts required
- Low noise, especially low pulsive noise
- SIP assures easy mounting on printed circuit board.

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM



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Nippon Electric Co.,Ltd.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Supply Voltage	V_{CC}	18	V
Package Dissipation	P_D	270*	mW
Operating Temperature	T_{opt}	-20 to +75	°C
Storage Temperature	T_{stg}	-40 to +125	°C

*Ta = 75°C

RECOMMENDED CONDITIONS (Ta = 25°C)

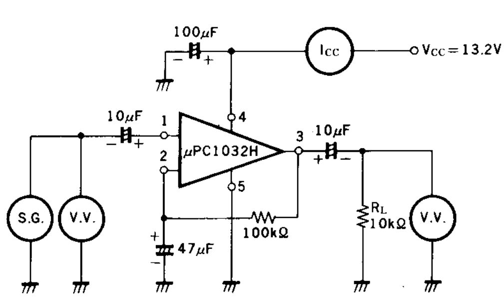
Operating Supply Voltage	V_{CC}	13.2	V
Supply Voltage Range	V_{CC}	8 to 17	V
Operating Ambient Temperature		-20 to +75	°C
Load impedance		10 kΩ TYP.	

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 13.2V, f = 1 kHz, R_L = 10 kΩ)

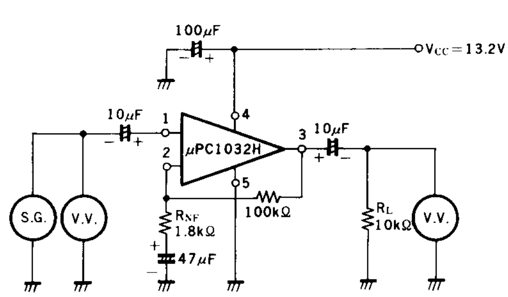
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CIRCUIT	TEST CONDITIONS
Circuit Current	I_{CC}		7	11.0	mA	①	v_{in} = 0
Open Loop Voltage Gain	A_{vo}	70	81		dB	①	v_o = 0.3V
Voltage Gain	A_v	33.5	35	35.5	dB	②	v_o = 0.3V, R_{NF} = 1.8 kΩ
Maximum Output Voltage	V_{OM}	1.1	1.7		V	③	T.H.D. = 1%, NAB ≒ 35 dB
Total Harmonic Distortion	T.H.D.		0.1	0.3	%	③	v_o = 0.3V, NAB ≒ 35 dB
Input Impedance	r_i	50	100		kΩ	③	
Equivalent Input Noise Voltage	v_{nin}		1.4	2.0	μVr.m.s.	④	R_G = 2.2kΩ, NAB ≒ 35dB
Cross Talk			-62		dB	⑤	v_o = 1V, (The other channel v_{in} = 0, R_G = 2.2kΩ)
Channel Balance		-0.3	0	+0.3	dB	⑤	v_o = 0.3V

TEST CIRCUITS

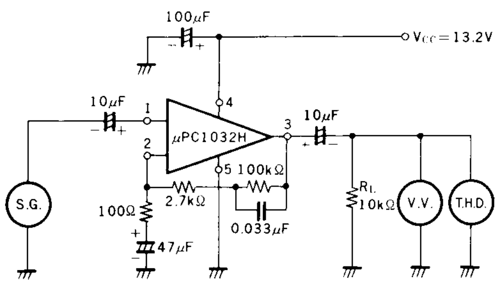
① I_{CC}, A_{vo} Test Circuit



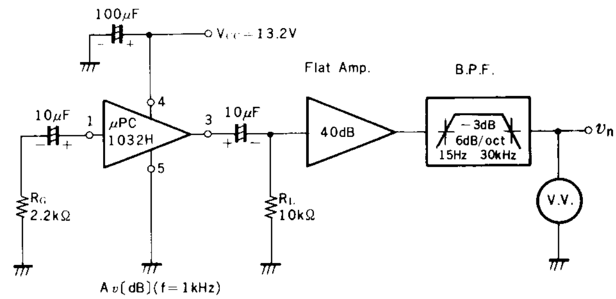
② A_v Test Circuit (for Ch. 1)



③ V_{OM}, T.H.D., r_i Test Circuit (for Ch. 1)

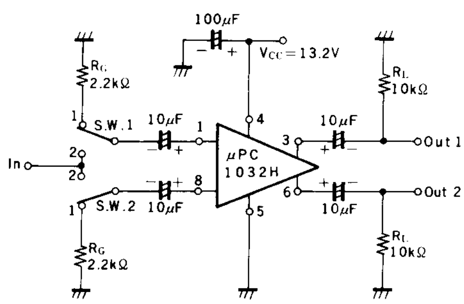


④ v_{nin} Test Circuit (for Ch. 1)



v_{nin} is calculated by v_n and amp. gain (A_v +40 dB).
External components of the IC are the same as the Test Circuit ③

⑤ **Cross Talk, Channel Balance Test Circuit**

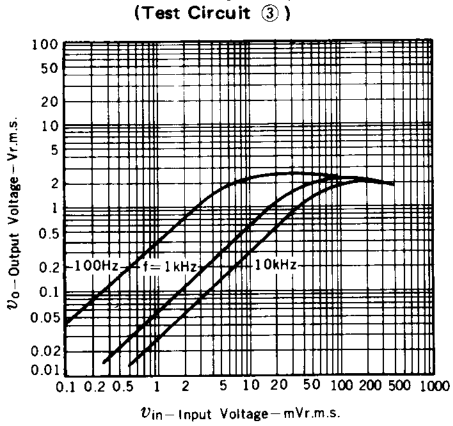


External Components of the IC are the same as the Test Circuit ③
Cross talk Test Procedure
- 20 log Out_2/Out_1
- Switch Position $SW_1 \rightarrow 2, SW_2 \rightarrow 1$
- 20 log Out_1/Out_2
- Switch Position $SW_1 \rightarrow 1, SW_2 \rightarrow 2$

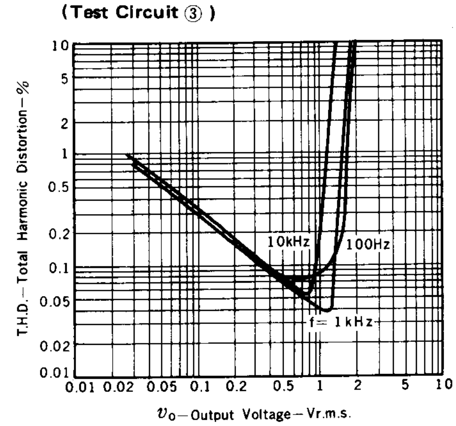
Channel Balance Test Procedure
- 20 log Out_1/Out_2
- Switch Position $SW_1 \rightarrow 2, SW_2 \rightarrow 2$

TYPICAL CHARACTERISTICS (Ta = 25°C)

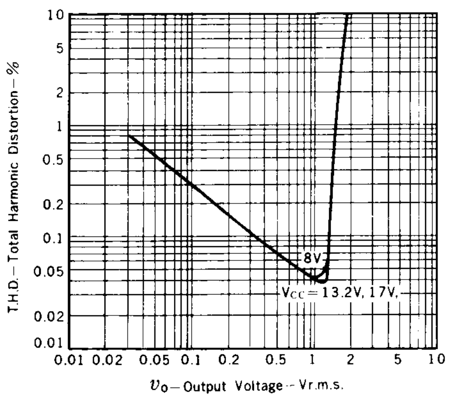
OUTPUT VOLTAGE vs. INPUT VOLTAGE (Test Circuit ③)



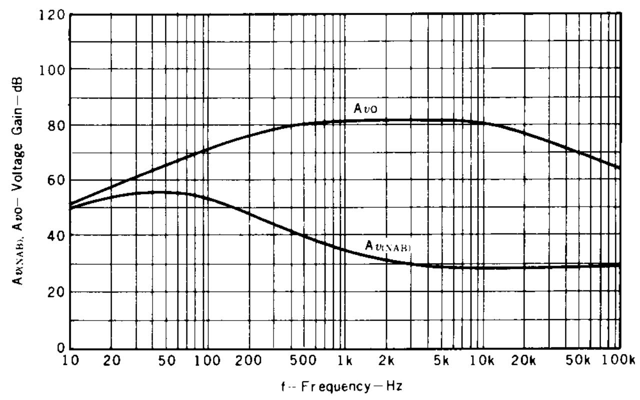
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE (Test Circuit ③)



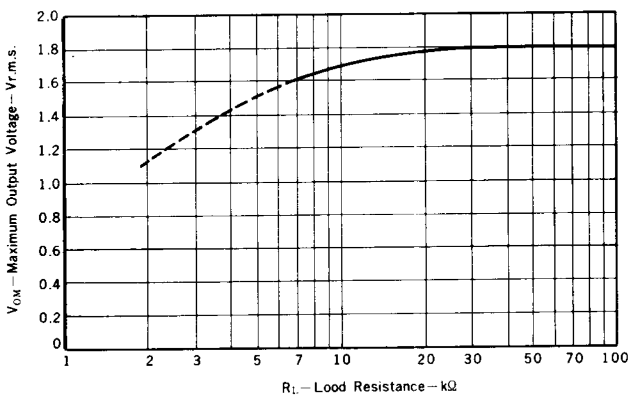
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE (Test Circuit ③)



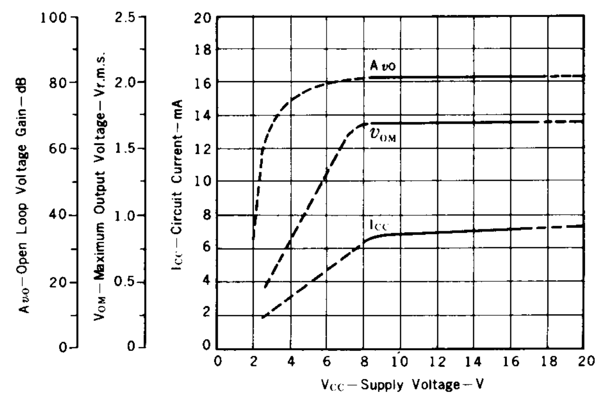
VOLTAGE GAIN vs. FREQUENCY (Test Circuit ①, ③)



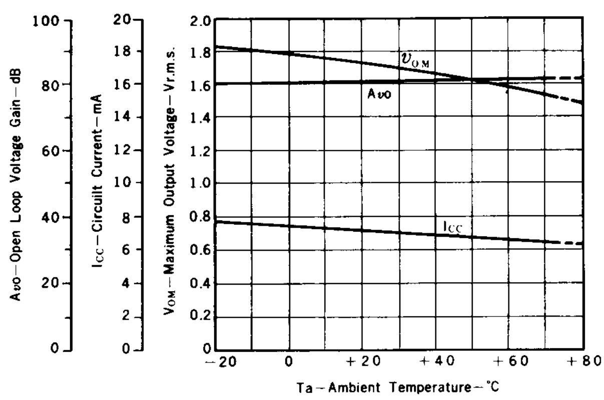
MAXIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE (Test Circuit ③)



CIRCUIT CURRENT, MAXIMUM OUTPUT VOLTAGE, OPEN LOOP VOLTAGE GAIN vs. SUPPLY VOLTAGE (Test Circuit ①, ③)

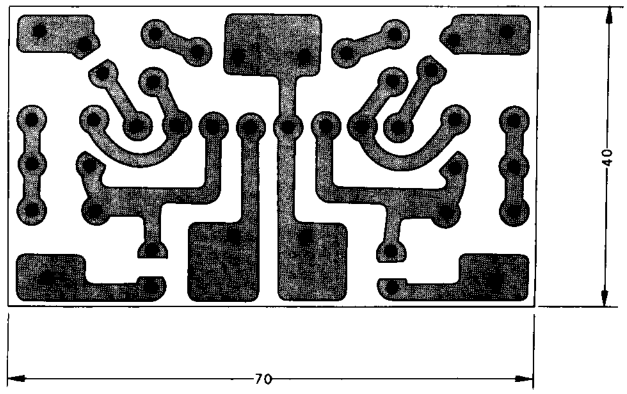


CIRCUIT CURRENT, MAXIMUM OUTPUT VOLTAGE, OPEN LOOP VOLTAGE GAIN AMBIENT TEMPERATURE (Test Circuit ①, ③)



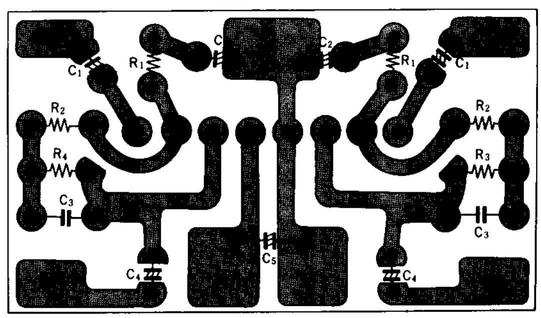
TYPICAL PRINTED CIRCUIT BOARD PATTERN

Bottom View (Unit : millimeters)



Components Layout

Foil Side



Components Side