μA2240

PROGRAMMABLE TIMER/COUNTER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

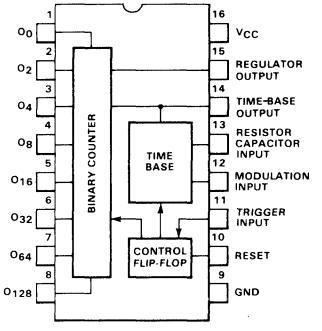
GENERAL DESCRIPTION – The μA2240 Programmable Timer/Counter is a monolithic controller capable of producing accurate microsecond to five day time delays. Long delays, up to three years, can easily be generated by cascading two timers. The timer consists of a time-base oscillator, programmable 8-bit counter and control flip-flop. An external resistor capacitor (RC) network sets the oscillator frequency and allows delay times from 1 RC to 255 RC to be selected. In the astable mode of operation, 255 frequencies or pulse patterns can be generated from a single RC network. These frequencies or pulse patterns can also easily be synchronized to an external signal. The trigger, reset and outputs are all TTL and DTL compatible for easy interface with digital system. The timer's high accuracy and versatility in producing a wide range of time delays makes it ideal as a direct replacement for mechanical or electromechanical devices.

- **ACCURATE TIMING FROM MICROSECONDS TO DAYS**
- **PROGRAMMABLE DELAYS FROM 1 RC TO 255 RC**
- **TTL, DTL AND CMOS COMPATIBLE OUTPUTS**
- **TIMING DIRECTLY PROPORTIONAL TO RC TIME CONSTANT**
- **HIGH ACCURACY – 0.5%**
- **EXTERNAL SYNC AND MODULATION CAPABILITY**
- **WIDE SUPPLY VOLTAGE RANGE**
- **EXCELLENT SUPPLY VOLTAGE REJECTION**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18 V
Output Current	10 mA
Output Voltage	18 V
Regulator Output Current	5 mA
Maximum Power Dissipation, Note 1	
Package Code D (Ceramic)	750 mW
Code P (Plastic)	650 mW
Operating Temperature Range Package	
Military (μA2240)	−55°C to +125°C
Commercial (μA2240C)	0°C to 70°C

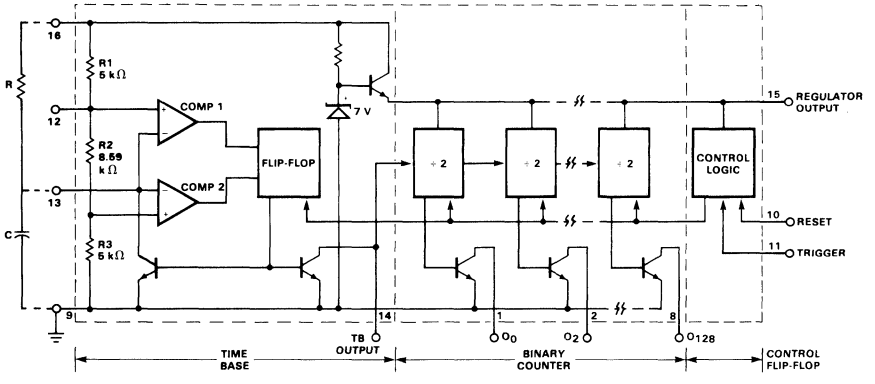
CONNECTION DIAGRAM
16-PIN DIP (TOP VIEW)
PACKAGE OUTLINES 7B, 9B
PACKAGE CODE D P



ORDER INFORMATION

TYPE	PART NO.
μA2240	μA2240DM
μA2240C	μA2240DC
μA2240C	μA2240PC

BLOCK DIAGRAM



NOTE 1: Above 25°C ambient derate linearly at 6.2 mW/°C for Package Code D and at 5.3 mW/°C for Package Code P.

ELECTRICAL CHARACTERISTICS: See Test Circuit Fig. 28, V_{CC} = 5 V, T_A = 25°C, R = 10 kΩ, C = 0.1 μF, unless otherwise noted

CHARACTERISTICS	CONDITIONS	μA2240			μA2240C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
GENERAL CHARACTERISTICS								
Supply Voltage	For $V_{CC} \leq$ 4.5 V, Short Pin 15 to Pin 16	4.0		15	4.0		15	V
Supply Current								
Total Circuit	V_{CC} = 5 V, V_{TR} = 0, V_{RS} = 5 V		3.5	6.0		4.0	7.0	mA
	V_{CC} = 15 V, V_{TR} = 0, V_{RS} = 5 V		12	16		13	18	mA
Counter Only	See Test Circuit, Figure 29		1			1.5		mA
Regulator Output, V_{Reg}	Measured at Pin 15, V_{CC} = 5 V	4.1	4.4		3.9	4.4		V
	V_{CC} = 15 V, See Test Circuit, Figure 30	6.0	6.3	6.6	5.8	6.3	6.8	V
TIME BASE SECTION								
Timing Accuracy (Note 2)	V_{RS} = 0, V_{TR} = 5 V		0.5	2.0		0.5	5.0	%
Temperature Drift	V_{CC} = 5 V, 0°C ≤ T_J ≤ 75°C		150	300		200		ppm/°C
	V_{CC} = 15 V		80			80		ppm/°C
Supply Drift	$V_{CC} \geq$ 8 V, See Figure 23		0.05	0.2		0.08	0.3	%/V
Max Frequency	R = 1 kΩ, C = 0.007 μF	100	130			130		kHz
Modulation Voltage Level	Measured at Pin 12 V_{CC} = 5 V	3.00	3.50	4.0	2.80	3.50	4.20	V
	V_{CC} = 15 V		10.5			10.5		V
Recommended Range of Timing Components	See Figure 20							
Timing Resistor, R		0.001		10	0.001		10	MΩ
Timing Capacitor, C		0.007		1000	0.01		1000	μF
TRIGGER/RESET CONTROLS								
Trigger	Measured at Pin 11, V_{RS} = 0							
Trigger Threshold			1.4	2.0		1.4	2.0	V
Trigger Current	V_{RS} = 0, V_{TR} = 2 V		8.0			10		μA
Impedance			25			25		kΩ
Response Time (Note 3)			1.0			1.0		μs
Reset	Measured at Pin 10, V_{TR} = 0							
Reset Threshold			1.4	2.0		1.4	2.0	V
Reset Current	V_{TR} = 0, V_{RS} = 2 V		8.0			10		μA
Impedance			25			25		kΩ
Response Time (Note 3)			0.8			0.8		μs
COUNTER SECTION	See Test Circuit, Figure 30							
Max Toggle Rate	V_{RS} = 0, V_{TR} = 5 V Measured at Pin 14	0.8	1.5			1.5		MHz
Input Impedance			20			20		kΩ
Input Threshold		1.0	1.4		1.0	1.4		V
Output:	Measured at Pins 1 through 8							
Rise Time	R_L = 3 kΩ, C_L = 10 pF		180			180		ns
Fall Time			180			180		ns
Sink Current	$V_{OL} \leq$ 0.4 V	3.0	5.0		2.0	4.0		mA
Leakage Current	V_{OH} = 15 V		0.01	8.0		0.01	15	μA

NOTES:
2. Timing error solely introduced by μA2240, measured as % of ideal time base period of T = 1.00 RC.
3. Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Pin 1.

FUNCTIONAL DESCRIPTION

(Figure 1 and Block Diagram, page 1)

When power is applied to the μA2240 with no trigger or reset inputs, the circuit starts with all outputs HIGH. Application of a positive-going trigger pulse to TRIG, pin 11, initiates the timing cycle. The Trigger input activates the time-base oscillator, enables the counter section and sets the counter outputs LOW. The time-base oscillator generates timing pulses with a period T = 1 RC. These clock pulses are counted by the binary counter section. The timing sequence is completed when a positive-going reset pulse is applied to R, pin 10.

Once triggered, the circuit is immune from additional trigger inputs until the timing cycle is completed or a reset input is applied. If both the reset and trigger are activated simultaneously, the trigger takes precedence.

Figure 2 gives the timing sequence of output waveforms at various circuit terminals, subsequent to a trigger input. When the circuit is in a Reset state, both the time-base and the counter sections are disabled and all the counter outputs are HIGH.

In most timing applications, one or more of the counter outputs are connected to the Reset terminal with S1 closed (*Figure 3*). The circuit starts timing when a trigger is applied and automatically resets itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the Reset terminal (switch S1 open), the circuit operates in an astable or free-running mode, following to a trigger input.

Important Operating Information

- Ground connection is pin 9.
- Reset R (pin 10) sets all outputs HIGH.
- Trigger TRIG (pin 11) sets all outputs LOW.
- Time-base TBO (pin 14) can be disabled by bringing the RC input (pin 13) LOW via a 1 k resistor.
- Normal Time-base Output TBO (pin 14) is a negative-going pulse greater than 500 ns.

  Note: Under the conditions of high supply voltages (V_{CC} > 7 V) and low values of timing capacitor (C < 0.1 μF, the pulse width of TBO may be too narrow to trigger the counter section. This can be corrected by connecting a 300 pF capacitor from TBO (pin 14) to ground (pin 9).
- Reset (pin 10) stops the time-base oscillator.
- Outputs $O_0 \ldots O_{128}$ (pins 1-8) sink 2 mA current with $V_{OL} \leq 0.4$ V.
- For use with external clock, minimum clock pulse amplitude should be 3 V, with greater than 1 μs pulse duration.

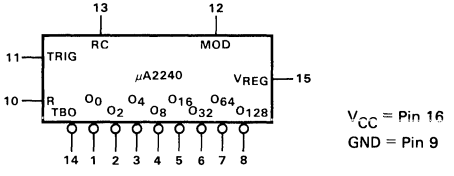


Fig. 1. Logic Diagram

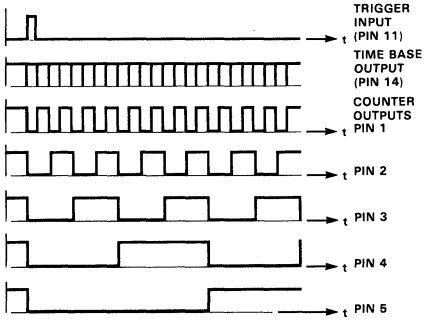


Fig. 2. Timing Diagram of Output Waveforms

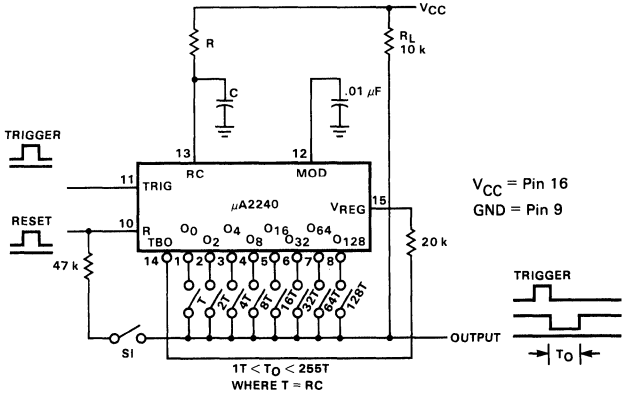


Fig. 3. Basic Circuit Connection for Timing Applications
Monostable: S1 Closed
Astable: S1 Open

CIRCUIT CONTROLS

Counter Outputs (O_0 . . . O_{128}, pins 1 thru 8)

The binary counter outputs are buffered open-collector type stages, as shown in the block diagram on page 1. Each output is capable of sinking 2 mA at 0.4 V V_{OL}. In the Reset condition, all the counter outputs are HIGH or in the non-conducting state. Following a trigger input, the outputs change state in accordance with the timing diagram of *Figure 2*. The counter outputs can be used individually, or can be connected together in a wired-OR configuration, as described in the Programming section.

Reset and Trigger Inputs (R and TRIG, pins 10 and 11)

The circuit is reset or triggered with positive-going control pulses applied to pins 10 and 11 respectively. The threshold level for these controls is approximately two diode drops (≈ 1.4 V) above ground. Minimum pulse widths for reset and trigger inputs are shown in *Figure 22*. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

Modulation and Sync Input (MOD, pin 12)

The oscillator time-base period, T, can be modulated by applying a dc voltage to MOD, pin 12 (see *Figure 25*). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to MOD, pin 12, as shown in *Figure 4*. Recommended sync pulse widths and amplitudes are also given.

The time base can be synchronized by setting the time-base period T to be an integer multiple of the sync pulse period, T_S. This can be done by choosing the timing components R and C at pin 13 such that:

$$T = RC = (T_S/m)$$

where

m is an integer, $1 \leq m \leq 10$

Figure 5 gives the typical pull-in range for harmonic synchronization for various values of harmonic modulus, m. For $m < 10$, typical pull-in range is greater than ±4% of time-base frequency.

RC Terminal (pin 13)

The time-base period T is determined by the external RC network connected to RC, pin 13. When the time base is triggered, the waveform at pin 13 is an exponential ramp with a period T = 1.0 RC.

Time-Base Output (TBO, pin 14)

The time-base output is an open-collector type stage as shown in the block diagram, page, 1, and requires a 20 kΩ pull-up resistor to pin 15 for proper circuit operation. In the Reset state, the time-base output is HIGH. After triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of *Figure 2*. The time-base output is internally connected to the binary-counter section and can also serve as the input for the external clock signal when the circuit is operated with an external time base. The counter section triggers on the negative-going edge of the timing or clock pulses generated at TBO, pin 14. The trigger threshold for the counter section is ≈ +1.4 V. The counter section can be disabled by clamping the voltage level at pin 14 to ground.

When using high supply voltages ($V_{CC} > 7$ V) and a small-value timing capacitor ($C < 0.1$ μF), the pulse width of the time-base output at pin 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 300 pF capacitor from pin 14 to ground.

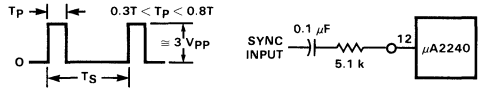


Fig. 4. Operation with External Sync. Signal

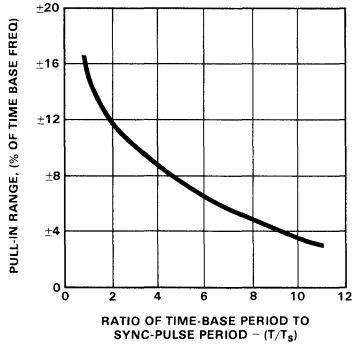


Fig. 5. Typical Pull-in Range for Harmonic Synchronization

Counter-Output Programming

The binary-counter outputs, $O_0 \ldots O_{128}$, pins 1 through 8 are open-collector type stages and can be shorted together to a common pull-up resistor to form a wired-OR connection; the combined output will be LOW as long as any one of the outputs is LOW. The time delays associated with each counter output can be added together. This is done by simply shorting the outputs together to form a common output bus as shown in *Figure 3*. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, is 32 T. Similarly, if pins 1, 5, and 6 are shorted to the output bus, the total time delay is $T_O = (1 + 16 + 32)\,T = 49\,T$. In this manner, by proper choice of counter terminals connected to the output bus, the timing cycle can be programmed to be $1\,T \leqslant T_O \leqslant 255\,T$.

Ultra Long Time-Delay Application

Two μA2240 units can be cascaded as shown in *Figure 6* to generate extremely long time delays. Total timing cycle of two cascaded units can be programmed from $T_O = 256$ RC to $T_O = 65{,}536$ RC in 256 discrete steps by selectively shorting one or more of the counter outputs from Unit 2 to the output bus. In this application, the Reset and the Trigger terminals of both units are tied together and the Unit 2 time base is disabled. Normally, the output is HIGH when the system is reset. On triggering, the output goes LOW where it remains for a total of $(256)^2$ or 65,536 cycles of the time-base oscillator.

In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption by using the circuit connection of *Figure 7*. In this case, the V_{CC} terminal (pin 16) of Unit 2 is left open, and the second unit is powered from the regulator output of Unit 1 by connecting the V_{REG} (pins 15) of both units together.

ASTABLE OPERATION

The μA2240 can be operated in its astable or free-running mode by disconnecting the Reset terminal (pin 10) from the counter outputs. Two typical circuits are shown in *Figures 8* and *9*. The circuit in *Figure 8* operates in its free-running mode with external trigger and reset signals. It starts counting and timing following a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 10, the circuit reverts back to its Reset state. This circuit is essentially the same as that of *Figure 3* with the feedback switch S1 open.

The circuit of *Figure 9* is designed for continuous operation. It self-triggers automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely. in astable or free-running operation, each of the counter outputs can be used individually as synchronized oscillators, or they can be interconnected to generate complex pulse patterns.

Binary Pattern Generation

In astable operation, as shown in *Figure 8*, the output of the μA2240 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of *Figure 2* which shows the phase relations between the counter outputs. *Figures 10* and *11* show some

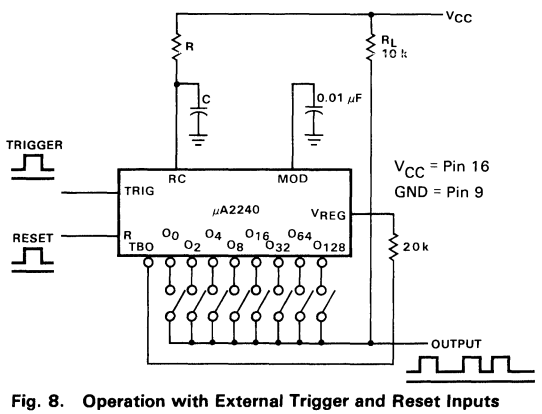


Fig. 8. Operation with External Trigger and Reset Inputs

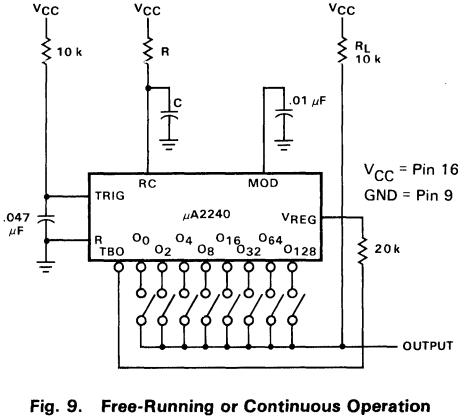


Fig. 9. Free-Running or Continuous Operation

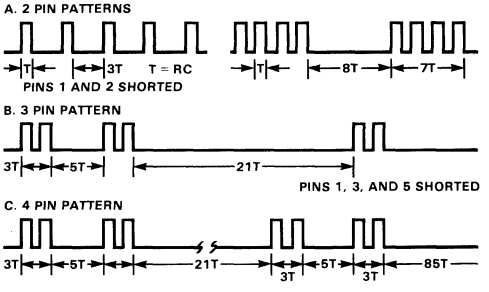


Fig. 10. Binary Pulse Patterns Obtained by Shorting Various Counter Outputs

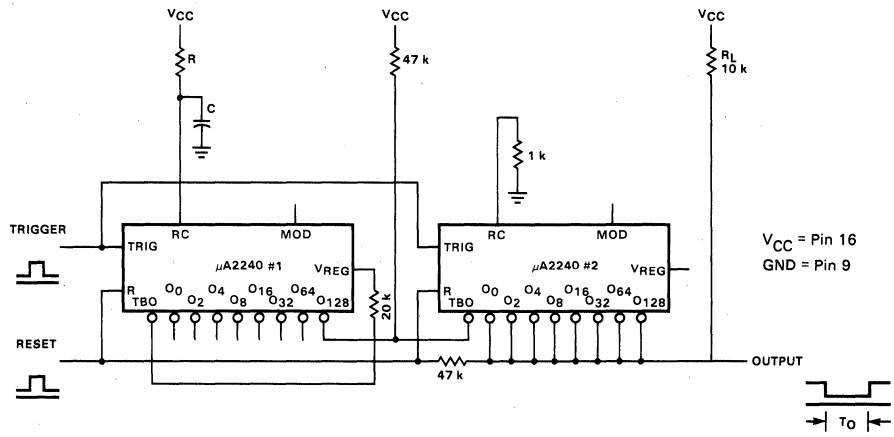


Fig. 6. Cascaded Operation for Long Delays

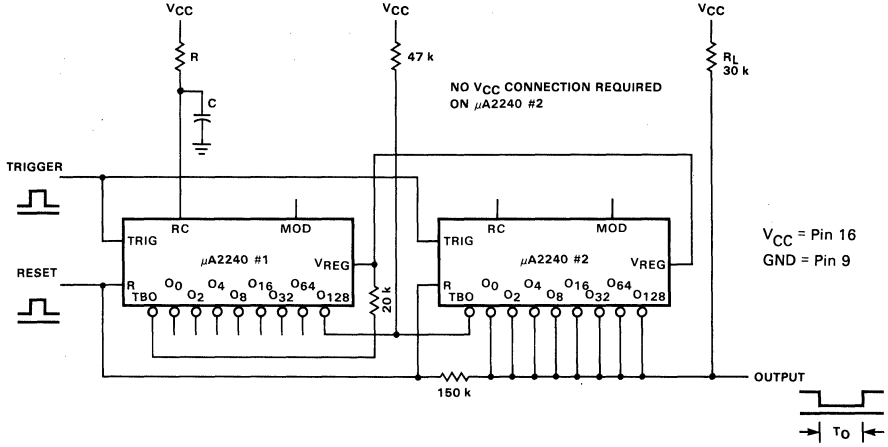


Fig. 7. Low Power Operation of Cascaded Timers

Regulator Output (V_{REG}, pin 15)
The regulator output V_{REG} is used internally to drive the binary counter and the control logic. This terminal can also be used as a supply to additional μA2240 circuits when several timer circuits are cascaded (see *Figure 7*) to minimize power dissipation. For circuit operation with an external clock, V_{REG} can be used as the V_{CC} input terminal to power down the internal time base and reduce power dissipation. When supply voltages less than 4.5 V are used with the internal time-base, pin 15 should be shorted to pin 16.

MONOSTABLE OPERATION

Precision Timing
In precision timing applications, the μA2240 is used in its monostable or self-resetting mode. The generalized circuit connection for this application is shown in *Figure 3*. The output is normally HIGH and goes LOW following a trigger input. It remains LOW for the time duration, T_O, and then returns to the HIGH state. The duration of the timing cycle T_O is given as:

$$T_O = NT = NRC$$

where T = RC is the time-base period as set by the choice of timing components at RC pin 13 (see *Figure 21*) and N is an integer in the range of $1 \leqslant N \leqslant 255$ as determined by the combination of counter outputs $O_0 \ldots O_{128}$, pins 1 through 8, connected to the output bus.

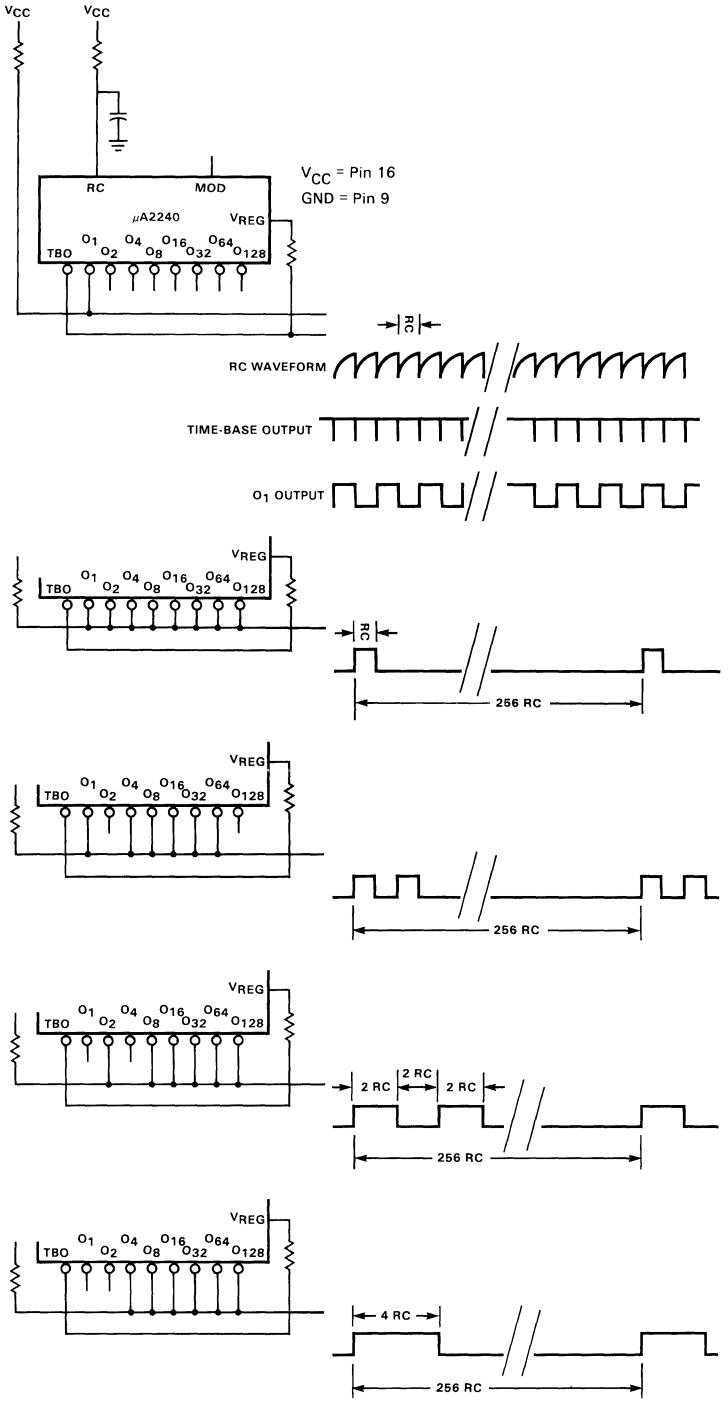


Fig. 11. Continuous Free-run Operation Examples of Output

of the complex pulse patterns that can be generated. The pulse pattern repeats itself at a rate equal to the period of the highest counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the lowest counter bit connected to the output.

OPERATION WITH EXTERNAL CLOCK

The μA2240 can be operated with an external clock or time base by disabling the internal time-base oscillator and applying the external clock input to TBO, pin 14. The recommended circuit connection for this application is shown in *Figure 12*. The internal time base is de-activated by connecting a 1 kΩ resistor from RC, pin 13, to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 V is required. Minimum external clock pulse width must be ⩾ 1 μs.

For low power operation with supply voltages of 6 V or less, the internal time base section can be powered down by connecting V_{CC} to pin 15 and leaving pin 16 open. In this configuration, the internal time base does not draw any current and the overall current drain is reduced by ≈ 3 mA.

FREQUENCY SYNTHESIZER

The programmable counter section of the μA2240 can be used to generate 255 discrete frequencies from a given time-base output setting using the circuit connection of *Figure 13*. The circuit output is a positive pulse train with a pulse width equal to T, and a period equal to (N + 1) T where N is the programmed count in the counter. The modulus N is the total count corresponding to the counter outputs connected to the output bus. For example, if pins 1, 3 and 4 are connected together to the output bus, the total count is N = 1 + 4 + 8 = 13; and the period of the output waveform is equal to (N + 1) T or 14 T. In this manner, 255 different frequencies can be synthesized from a given time-base setting.

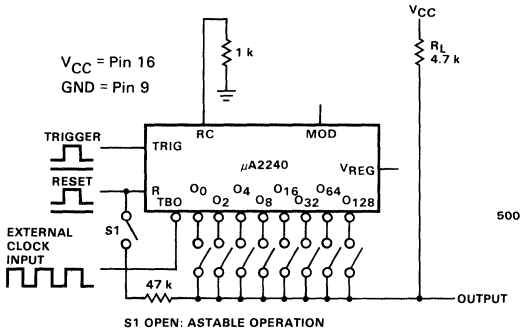


Fig. 12. Operation with External Clock

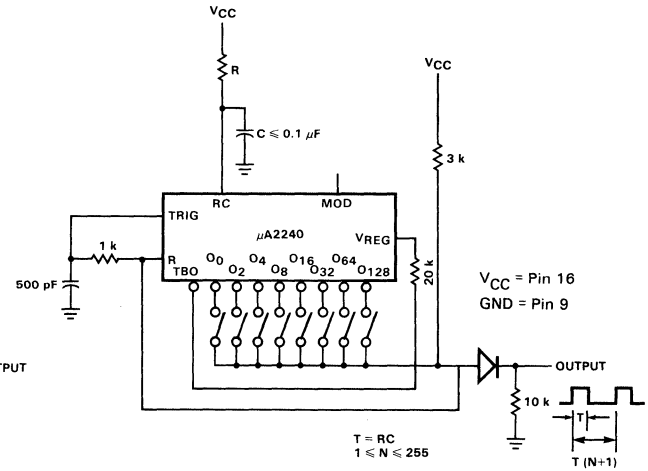


Fig. 13. Frequency Synthesis from Internal Time-Base

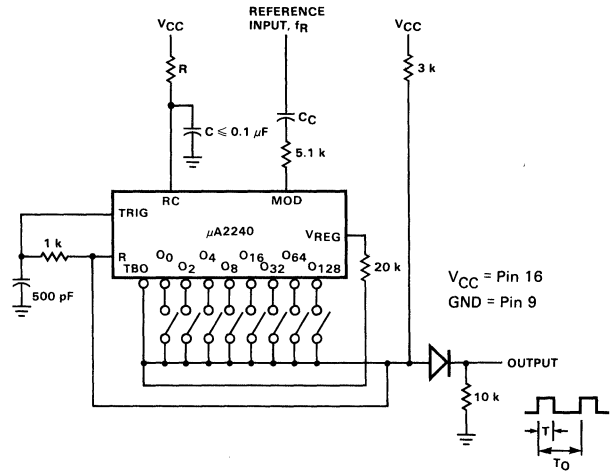


Fig. 14. Frequency Synthesis by Harmonic Locking to an External Reference

SYNTHESIS WITH HARMONIC LOCKING

The harmonic synchronization feature of the μA2240 time base can be used to generate a wide number of discrete frequencies from a given input reference frequency. The circuit connection for this application is shown in *Figure 14* (see *Figures 4* and *5* for external sync waveform and harmonic capture range). If the time base is synchronized to (m)th harmonic of input frequency where $1 \leqslant m \leqslant 10$, the frequency f_O of the output waveform in *Figure 14* is related to the input reference frequency f_R as

$$f_O = f_R \frac{m}{(N+1)}$$

where m is the harmonic number, and N is the programmed counter modulus. For a range of $1 \leqslant N \leqslant 255$, the circuit of *Figure 14* can produce 2550 different frequencies from a single fixed reference.

The circuit of *Figure 14* can be used to generate frequencies which are not harmonically related to a reference input. For example, by selecting the external RC to set m = 10 and setting N = 5, a 100 Hz output frequency synchronized to 60 Hz power line frequency can be obtained.

STAIRCASE GENERATOR

The μA2240 timer/counter can be interconnected with an external operational amplifier and a precision resistor ladder to form a staircase generator as shown in *Figure 15*. Under Reset condition, the output is LOW. When a trigger is applied, the op amp output goes HIGH and generates a negative-going staircase of 256 equal steps. The time duration of each step is equal to the time-base period T. The staircase can be stopped at any level by applying a disable signal to pin 14, through a steering diode, as shown in *Figure 15*. The count is stopped when pin 14 is clamped at a voltage level ⩽ 1.0 V.

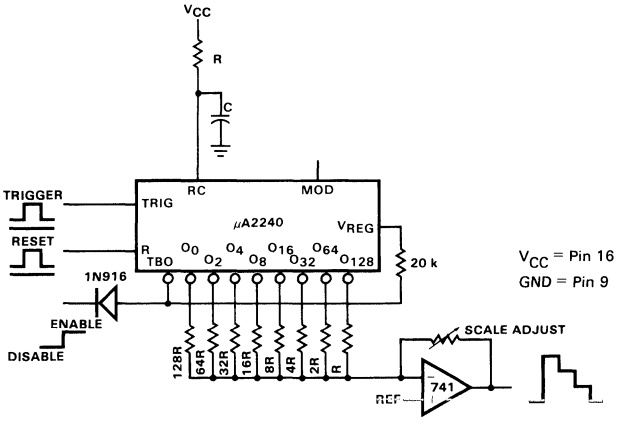


Fig. 15. Staircase Generator

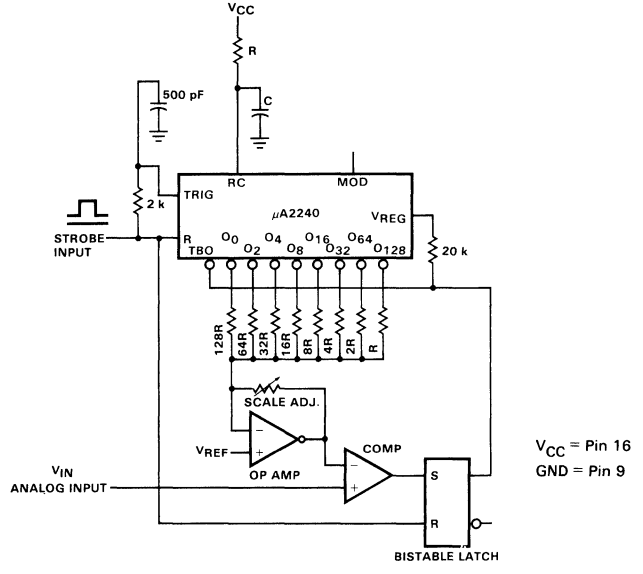


Fig. 16. Digital Sample and Hold Circuit

DIGITAL SAMPLE AND HOLD

Figure 16 shows a digital sample and hold circuit using the μA2240. Circuit operation is similar to the staircase generator described in the previous section. When a strobe input is applied, the RC low-pass network between the Reset and the Trigger inputs resets the timer, then triggers it. This strobe input also sets the output of the bistable latch to a HIGH state and activates the counter.

The circuit generates a staircase voltage at the op amp output. When the level of the staircase reaches that of the analog input to be sampled, the comparator changes state, activates the bistable latch and stops the count. At this point, the voltage level at the op amp output corresponds to the sampled analog input. Once the input is sampled, it is held until the next strobe signal. Minimum recycle time of the system is ≈ 6 ms.

ANALOG-TO-DIGITAL CONVERTER

Figure 17 shows a simple 8-bit A/D converter system using the μA2240. Circuit operation is very similar to that of the digital sample and hold system of *Figure 16*. In the case of A/D conversion, the digital output is obtained in parallel format from the binary-counter outputs with the output at pin 8 corresponding to the most significant bit (MSB). Recycle time is ≈ 6 ms.

DIGITAL TACHOMETER TIME BASE

A digital tachometer requires a time-base generator to supply two pulse outputs at specific intervals, *e.g.*, every second. The first pulse is a command (load) to transfer the accumulated counts in the counter section into latches (memory); the second resets the counter to zero. A simple adjustable time base, accurate to approximately ±0.5%, can be implemented using the circuit in *Figure 18*.

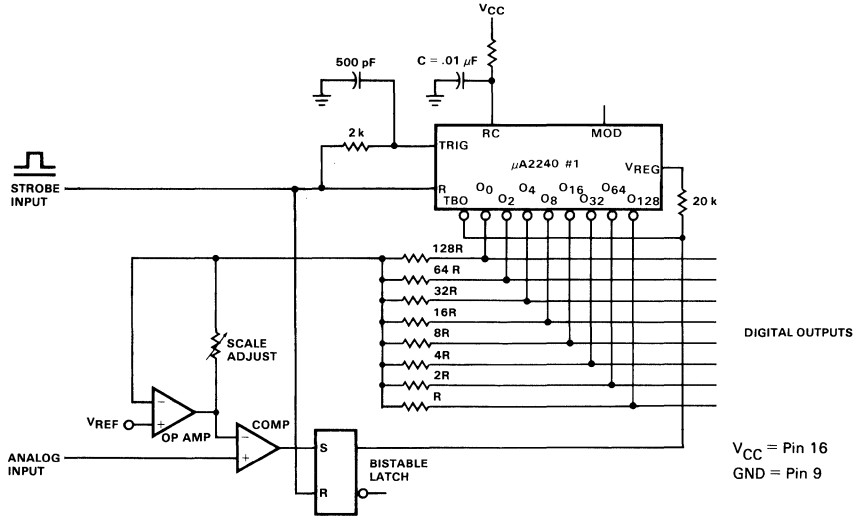


Fig. 17. Analog-to-Digital Converter

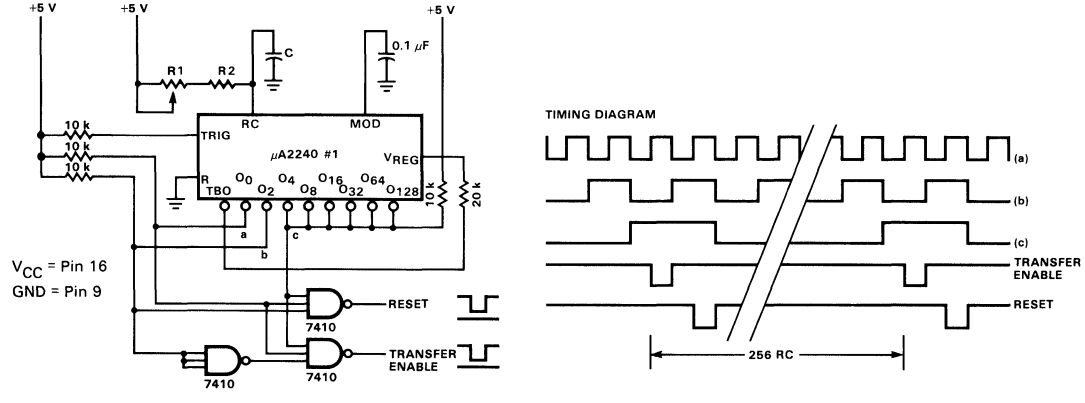


Fig. 18. Simple Time Generator for a Digital Tachometer

TYPICAL ELECTRICAL CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE IN RESET CONDITION

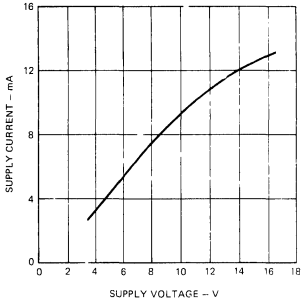


Fig. 19

RECOMMENDED RANGE OF TIMING COMPONENT VALUES

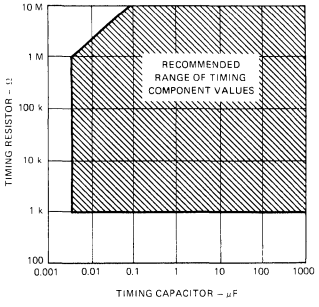


Fig. 20

TIME BASE PERIOD AS A FUNCTION OF EXTERNAL RC

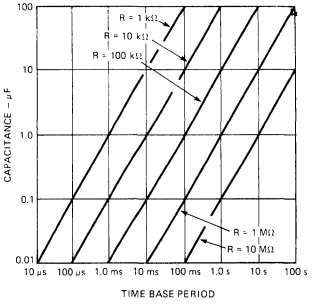


Fig. 21

MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AND RESET AMPLITUDE

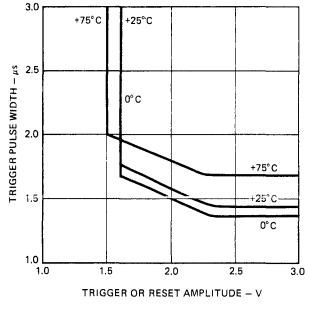


Fig. 22

TIME BASE PERIOD DRIFT AS A FUNCTION OF SUPPLY VOLTAGE

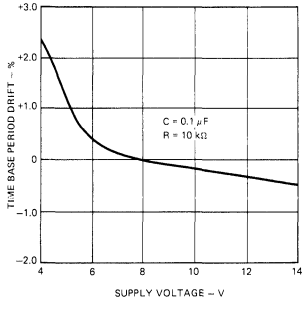


Fig. 23

MINIMUM TRIGGER/RETRIGGER TIMING AS A FUNCTION OF TIMING CAPACITOR

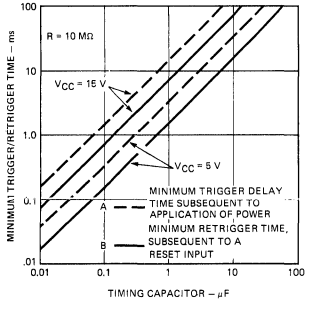


Fig. 24

NORMALIZED CHANGE IN TIME BASE PERIOD AS A FUNCTION OF MODULATION VOLTAGE

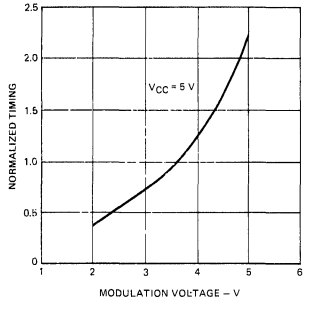


Fig. 25

TIME BASE PERIOD AS A FUNCTION OF TEMPERATURE

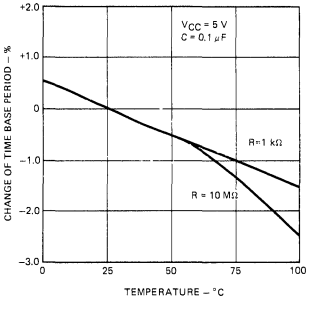


Fig. 26

TIME BASE PERIOD AS A FUNCTION OF TEMPERATURE

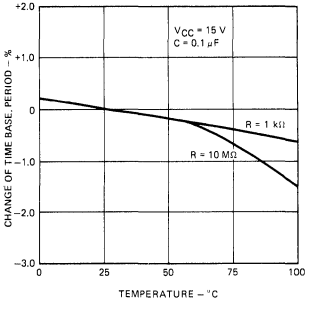


Fig. 27

7

TEST CIRCUITS

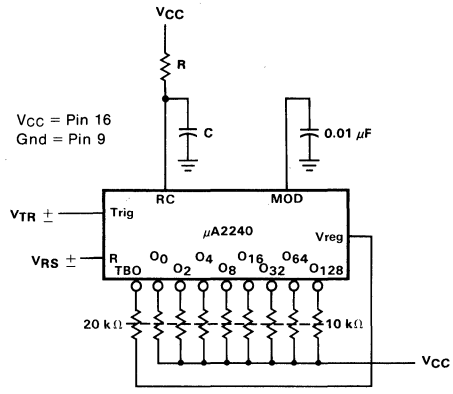


Fig. 28. Generalized Test Circuit

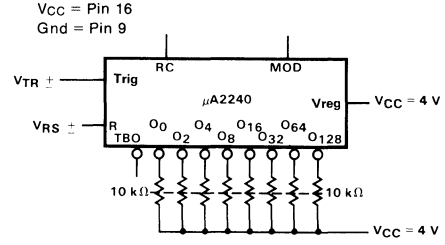


Fig. 29. Test Circuit for Low Power Operation (Time Base Powered Down)

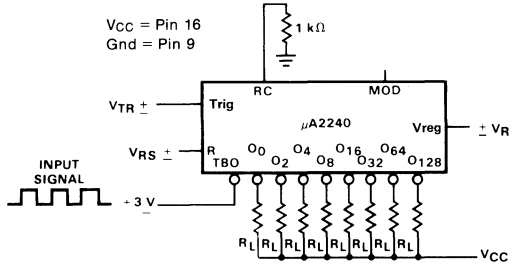


Fig. 30. Test Circuit for Counter Section