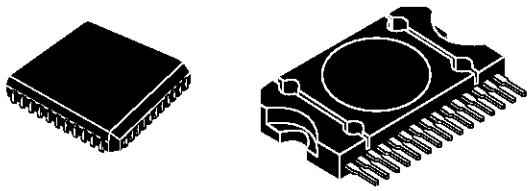
SGS-THOMSON MICROELECTRONICS

L3000S
L3030

SUBSCRIBER LINE INTERFACE KIT

PRELIMINARY DATA

- PROGRAMMABLE DC FEEDING RESIS-TANCE AND LIMITING CURRENT (four values available)
- THREE OPERATING MODES : STAND-BY, CONVERSATION, RINGING
- NORMAL/BOOST BATTERY, DIRECT/REVERSE POLARITY
- SIGNALLING FUNCTION (off-hook/GND-key)
- FILTERED OFF-HOOK DETECTION IN STAND-BY (10ms)
- QUICK OFF-HOOK DETECTION IN CONVERSATION (< 1ms) FOR LOW DIAL PULSE DETECTION DISTORTION
- HYBRID FUNCTION
- RINGING GENERATION WITH QUASI ZERO OUTPUT IMPEDANCE, ZERO CROSSING INJECTION (no ext. relay needed) AND RING TRIP DETECTION
- AUTOMATIC RINGING STOP WHEN OFF-HOOK IS DETECTED
- PARALLEL AND SERIAL DIGITAL INTERFACES
- TELETAXE SIGNAL INJECTION ($2V_{RMS}/5V_{RMS}$)
- LOW NUMBER OF EXTERNAL COMPONENTS
- GOOD REJECTION OF THE NOISE ON BATTERY VOLTAGE (20dB at 10Hz and 35dB at 1kHz)
- POSSIBILITY TO WORK ALSO WITH HIGH COMMON MODE CURRENTS
- INTEGRATED THERMAL PROTECTION WITH THERMAL OVERLOAD INDICATION
- SURFACE MOUNT PACKAGE (PLCC44 + PowerSO-20)



PLCC44 **FLEXIWATT15**

PowerSO20

slug-up **slug-down**

ORDERING NUMBERS :

L3030 (PLCC44)
L3000SX-VM (FLEXIWATT15)
L3000SX (PowerSO20 slug-up)
L3000SX-77 (PowerSO20 slug-down)

DESCRIPTION

The ST SLIC KIT (L3000S/L3030) is a set of solid state devices designed to integrate main of the functions needed to interface a telephone line. It consists of 2 integrated devices : the L3000S line interface circuit and the L3030 control unit.

This kit performs the main features of the BORSHT functions :

- Battery feed
- Ringing
- Signalling
- Hybrid

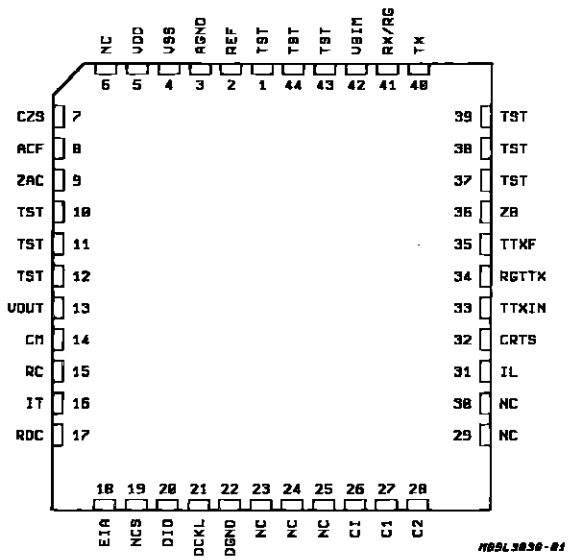
Additional functions, such as battery reversal, extra battery use, line overvoltage sensing and metering-pulse injection are also featured ; most external characteristics, as AC and DC impedances, are programmable with external components. The SLIC injects ringing in balanced mode and for that, as well as for the operation in battery boosted, a positive battery voltage shall be available on the subscriber card. As the right ringing signal amplification both in voltage and in current is provided by SLIC, the ring signal generator shall only provide a low level signal (0.285Vrms).

This kit is fabricated using a 140V Bipolar technology for L3000S and a 12V Bipolar I^2L technology for L3030.

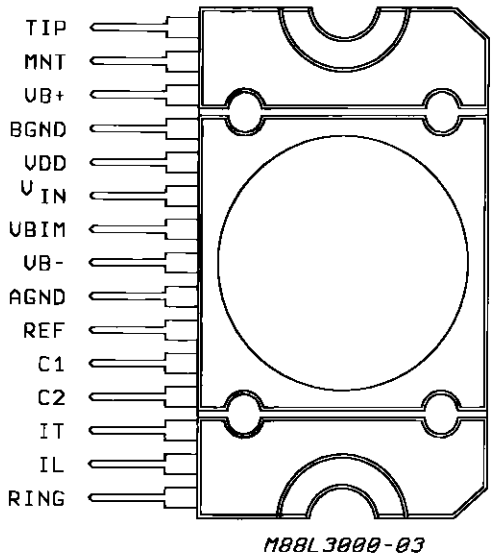
L3030 is available PLCC44 and L3000S in both FLEXIWATT15 and PowerSO-20 for surface mount application.

This kit is suitable for all the following applications: C.O. (Central Office), DLC (Digital Loop Carrier) and high range PABX (Private Automatic Branch Exchange).

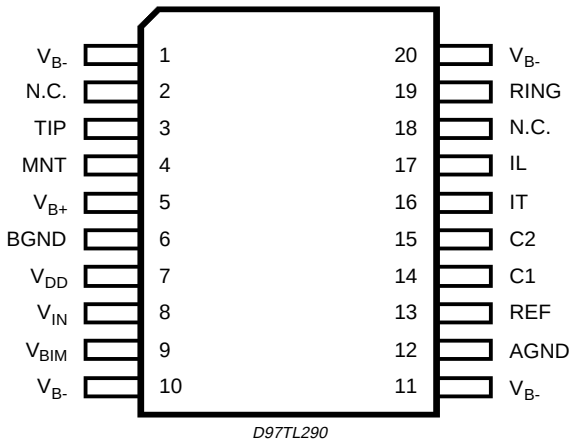
PIN CONNECTIONS (top view)



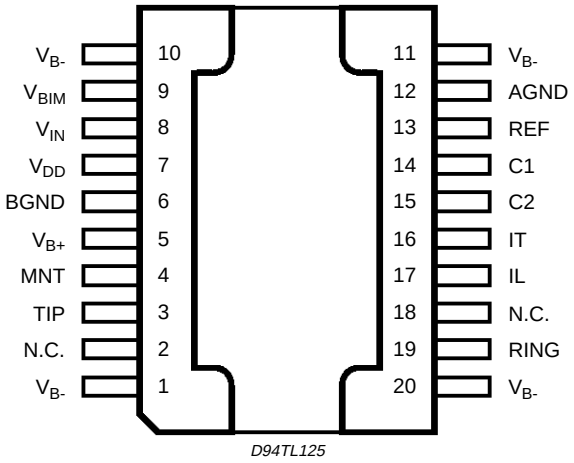
PLCC44



FLEXIWATT15



PowerSO-20 (slug-down)



PowerSO-20 (slug-up)

PIN DESCRIPTION (L3000S)

FLEX. N°	PSO N°	Name	Description
1	3	TIP	A line termination output with current capability up to 100mA (I_a is the current sourced from this pin).
2	4	MNT	Positive Supply Voltage Monitor
3	5	V_B+	Positive Battery Supply Voltage
4	6	BGND	Battery ground relative to the V_B+ and the V_B– supply voltages. It is also the reference ground for TIP and RING signals.
5	7	V_{DD}	Positive Power Supply + 5V
6	8	VIN	2 wire unbalanced voltage input.
7	9	VBIM	Output voltage without current capability, with the following functions : - give an image of the total battery voltage scaled by 40 to the low voltage part. - filter by an external capacitor the noise on V_B–.
8	1, 10 11, 20	V_B–	Negative Battery Supply Voltage
9	12	AGND	Analog Ground. All input signals and the V_{DD} supply voltage must be referred to this pin.
10	13	REF	Voltage reference output with very low temperature coefficient. The connected resistor sets internal circuit bias current.
11	14	C1	Digital signal input (3 levels) that defines device status with pin 12.
12	15	C2	Digital signal input (3 levels) that defines device status with pin 11.
13	16	I_T	High precision scaled transversal line current signal. $I_T = \frac{I_a + I_b}{100}$
14	17	I_L	Scaled longitudinal line current signal. $I_L = \frac{I_b - I_a}{100}$
15	19	RING	B line termination output with current capability up to 100mA (I_b is the current sunk into this pin).
–	2, 18	N.C.	Not connected

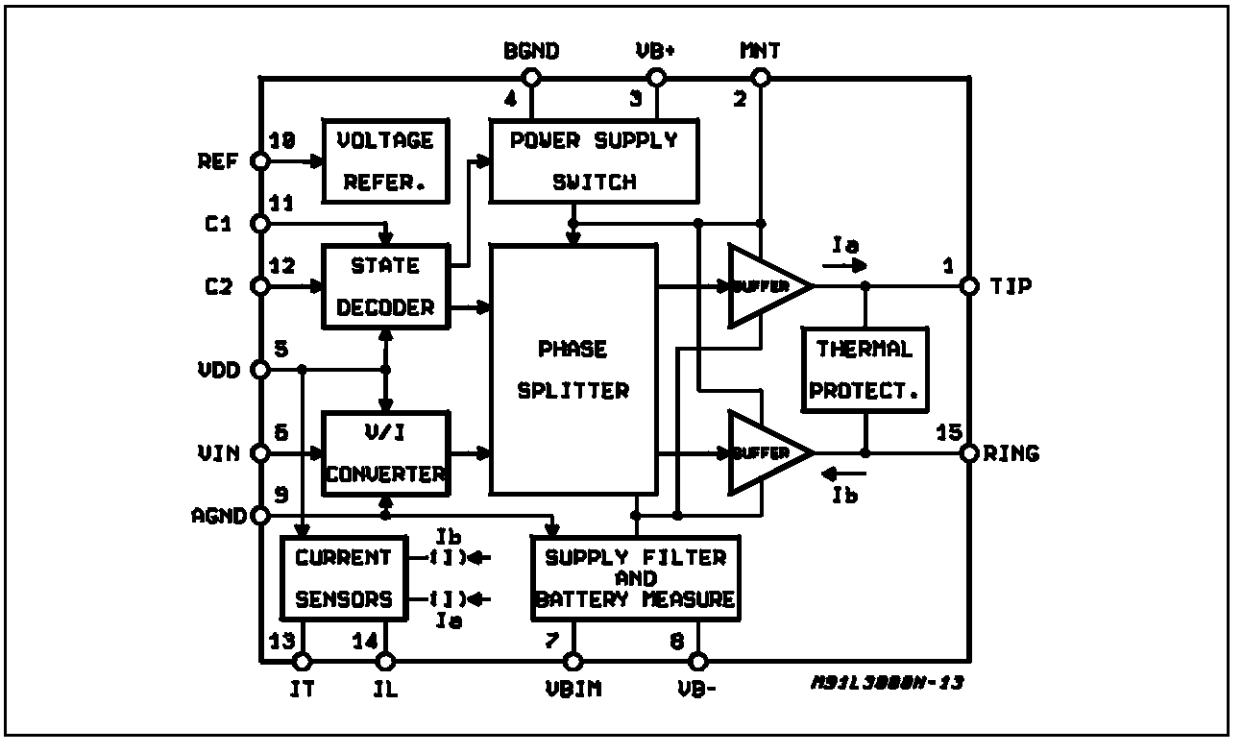
Notes: 1) Unless otherwise specified all the diagrams in this datasheet refers to the FLEXIWATT15 pin connection.

2) All informations relative to the PowerSO-20 package option should be considered as advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

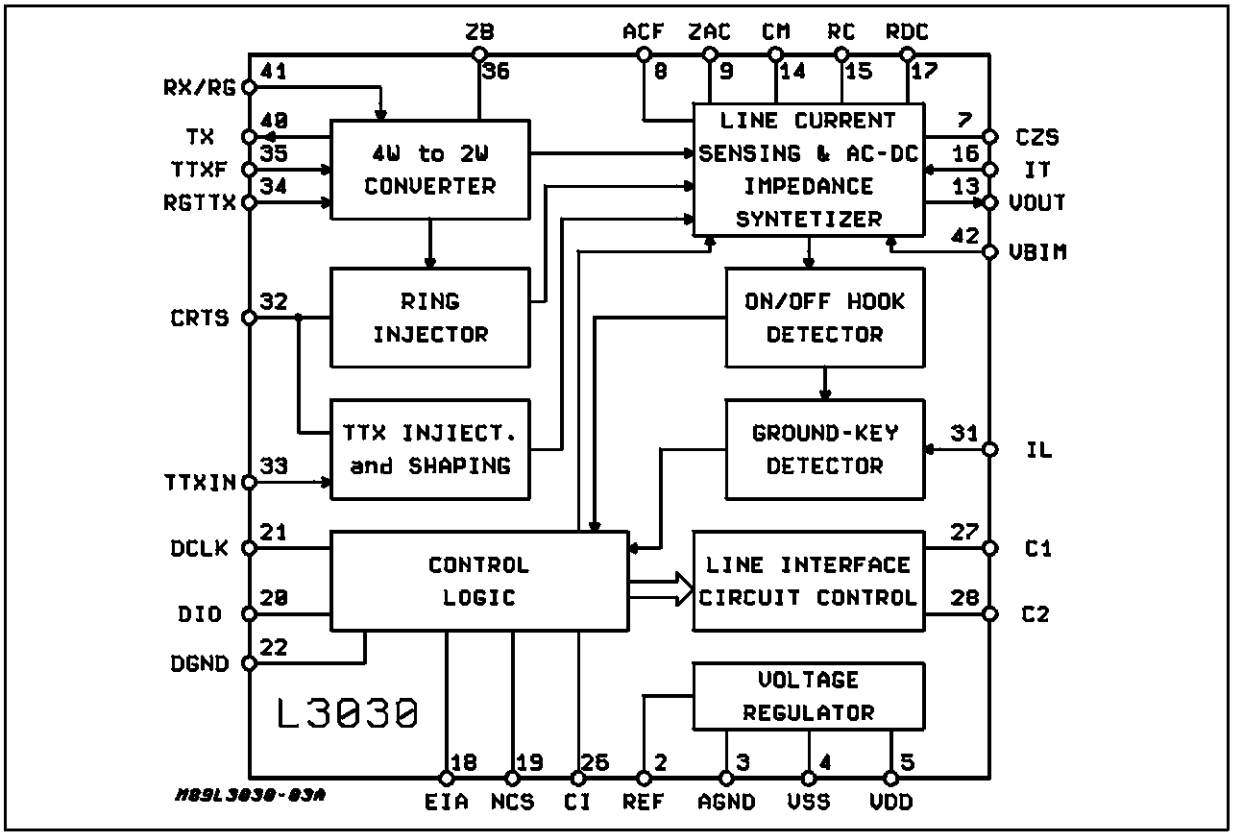
PIN DESCRIPTION (L3030)

Pin	Symbol	Function
1	TST	This pin is connected internally for test purpose. It should not be used as a tie point for external components.
2	REF	Bias Set
3	AGND	Analog Ground
4	VSS	– 5V
5	VDD	+ 5V
6	N.C.	Not connected.
7	CZS	AC Feedback Input
8	ACF	AC Line Impedance Synthesis
9	ZAC	AC Impedance Adjustement
10 11 12	TST	These pins are connected internally for test purpose. It should not be used as a tie point for external components.
13	VOUT	Two wire unbalanced output.
14	CM	Capacitor Multiplier Input
15	RC	DC Feedback Input
16	IT	Transversal Line Current
17	RDC	DC Feeding System
18	EIA	Read/write Command
19	NCS	Chip Select Command
20	DIO	Data Input/output
21	DCKL	Clock Signal
22	DGND	Digital Ground
23	N.C.	Not connected.
24	N.C.	Not connected.
25	N.C.	Not connected.
26	CI	Input/output Changing Command
27	C1	State Control Signal 1
28	C2	State Control Signal 2
29	N.C.	Not connected.
30	N.C.	Not connected.
31	IL	Longitudinal Line Current
32	CRTS	Ringtrip Det. & TTX Shaping
33	TTXIN	Teletaxe Signal Input
34	RGTTX	TTX Filter Level Compensation
35	TTXF	TTX Filter Input
36	ZB	Balancing Network
37 38 39	TST	These pins are connected internally for test purpose. It should not be used as a tie point for external components.
40	TX	4W Sending Output
41	RX/RG	4W Receiving and Ring Input
42	VBIM	Battery Image Input
43 44	TST	These pins are connected internally for test purpose. It should not be used as a tie point for external components.

L3000S BLOCK DIAGRAM



L3030 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_b–	Negative Battery Voltage	– 80	V
V_b+	Positive Battery Voltage	80	V
$\|V_b–\| + \|V_b+\|$	Total Battery Voltage	140	V
V_{dd}	Positive Supply Voltage	+ 6	V
V_{ss}	Negative Supply Voltage	– 6	V
$V_{agnd} – V_{bgnd}$	Max. Voltage between Analog Ground and Battery Ground	5	V
T_j	Max. Junction Temperature	+ 150	°C
T_{stg}	Storage Temperature	– 55 to + 150	°C

THERMAL DATA

Symbol	Parameter	Value		Unit
L3000S HIGH VOLTAGE		**Flexiwatt**	**PWSO20**	
$R_{th\ j\text{-}case}$	Thermal Resistance Junction to Case	Max. 4	Typ. 2	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	Max. 50	Max. 60	°C/W
L3030 LOW VOLTAGE				
$R_{th\ j\text{-}amb}$	Max. Resistance Junction to Ambient	80		°C/W

OPERATING RANGE

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{oper}	Operating Temperature Range	0		70	°C
V_b–	Negative Battery Voltage	– 70	– 48	– 24	V
V_b+	Positive Battery Voltage	0	+ 72	+ 75	V
$V_b– + V_b+$	Total Battery Voltage		120	130	V
V_{dd}	Positive Supply Voltage	+ 4.5		+ 5.5	V
V_{ss}	Negative Supply Voltage	– 5.5		– 4.5	V
I_{max}	Total Line Current (IL + IT)			85	mA

FUNCTIONAL DESCRIPTION

L3000S - High Voltage Circuit

The L3000S line interface provides a battery feeding for telephone lines and ringing injection. The IC contains a state decoder that under external control can force the following operational modes : stand-by, conversation and ringing.

In addition Power down mode can be forced connecting the bias current resistor to V_{DD} or leaving it open.

Two pins, I_L and I_T, carry out the information concerning line status which is detected by sensing the line current into the output stage.

The L3000S amplifies both the AC and DC signals entering at pin 6 (VIN) by a factor equal to 40.

Separate grounds are provided :
- Analog ground as a reference for analog signals
- Battery ground as a reference for the output stages

The two ground should be shorted together at a low impedance point.

L3030 - Control Unit

The L3030 low voltage control unit controls L3000S line interface module, giving the proper information to set line feed characteristic, to inject ringing and TTX signal and synthetizes the line and balance impedances. An on chip digital interface allows a microprocessor to control all the operations. L3030 defines working states of line interface and also informs the card controller about line status.

L3000S - Working States

In order to carry out the different possible operations, the L3000S has several different working states. Each state is defined by the voltage respectively applied by pins 27 and 28 of L3030 to the pins 11 and 12 of L3000S.

Three different voltage levels (– 3, 0, + 3) are available at each connection, so defining nine possible

Table 1.

		Pin 28 of L3030 / Pin 12 of L3000S (C2)		
		+ 3	0	– 3
Pin 27 of L3030 / Pin 11 of L3000S	+ 3	Stand-by	Conversation in Normal Battery Direct Polarity	Conversation in Normal Battery Reverse Polar
	0	Not allowed.	Conversation in Boost Battery Direct Polarity	Conversation in Boost Battery Reverse Polar
	– 3	Not allowed.	Ringing with Direct Polarity	Not allowed.

states as listed in Table. 1.

Appropriate combinations of two pins define the three modes of the ST SLIC, that are :

a) Stand-by (SBY)
b) Conversation (CVS), Normal and Reverse polarity
c) Ringing (RING)
d) Boost Battery (BB), Normal and Reverse polarity

A fifth status, Power down (PD), can be set disconnecting the bias resistor (RH) from pin 10 of L3000S by means of an external transistor.

The main difference between Stand-by and Power down is that in SBY the power consumption on the voltage battery VB– (– 48V) is reduced but the L3000S DC feeding and monitoring circuits are still active. In PD the power consumption on VB- is reduced to zero, and the L3000S is completely switched off.

The SBY status should be used when the telephone is in On hook and PD status only in emergency condition when it is mandatory to cut any possible dissipation but no operation are requested.

OPERATING MODES

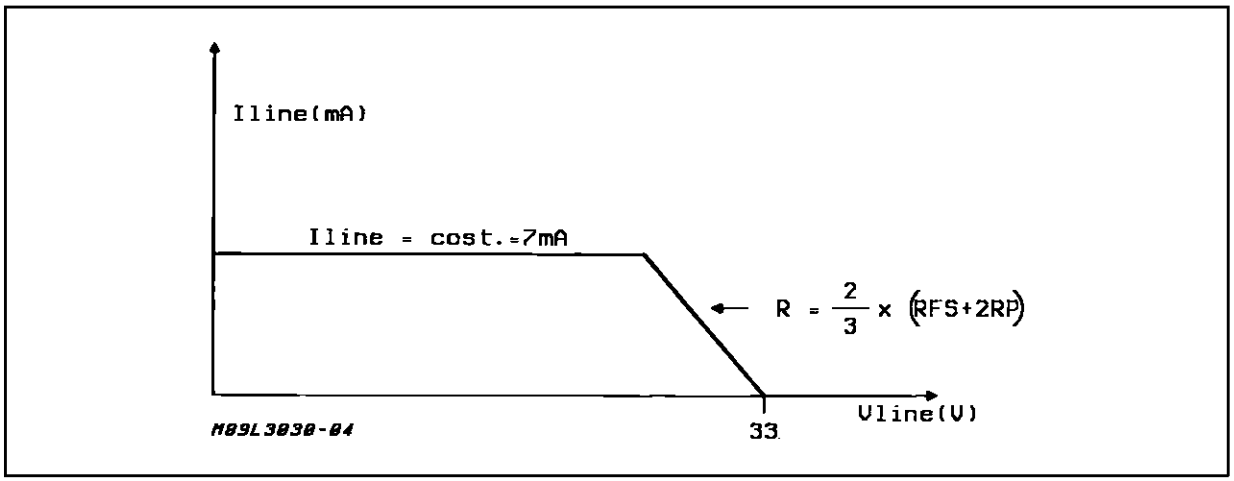
Stand-by (SBY) Mode

In this mode, the bias currents of both L3000S and L3030 are reduced as only some parts of the two circuits are completely active, control interface and current sensors among them. The current supplied to the line is limited at 7mA, and the slope of the DC characteristic corresponds to :

$$R = \frac{2}{3} \times (RFS + 2RP)$$

The Line voltage in on Hook condition is just the battery voltage minus the voltage drop (approx. 15V) of the output stage amplifiers (see Fig. 1).

Figure 1 : DC Characteristics in Stand-by Mode.



The AC characteristic is just the resistance of the two serial resistors RP.

In Stand-by mode the battery polarity is just in direct condition, that is the TIP wire more positive than the RING one ; boost battery is not achievable. There are two possible line conditions where the SLIC is expected to be in stand-by mode :

1) ON-HOOK (I_{line} < 5mA). Normal on-hook condition.
2) OFF-HOOK (I_{line} > 7mA). Handset is unhooked, the SLIC is waiting for command to activate conversation.

When the SLIC is in stand-by mode, the power dissipation of L3000S does not exceed 120mW (from -48V) eventually increased of a certain amount if some current is flowing into the line.

The power dissipation of L3030 in the same condition, is typically 120mW.

The Stand-by Mode is set when the byte sent to the L3030 Serial Digital Interface has the first two bits (BIT0R and BIT1R) equal to "0".

Setting to 0 all the 8 bits of the command sent to the digital interface of L3030, the bias currents of both L3000S and L3030 are reduced and only some parts of the two circuits are active similarly to the stand-by mode ; in this situation, named power-down denial, the line sensors are disabled (ON/OFF-HOOK line conditions cannot be recognized) and the current supplied to the line is limited at 0.25mA.

Conversation (CVS) or Active Mode

In conversation mode it is possible to select between two different DC Characteristics by the BIT5R of the Serial Interface.

1) Normal Battery (NB)
2) Boost Battery (BB)

It is also possible to select (BIT4R) the polarity of the DC line voltage and (BIT6R-BIT7R) one of the four values of limiting current (25mA or 30mA or 45mA or 70mA).

Battery reverse can take place either before or during conversation.

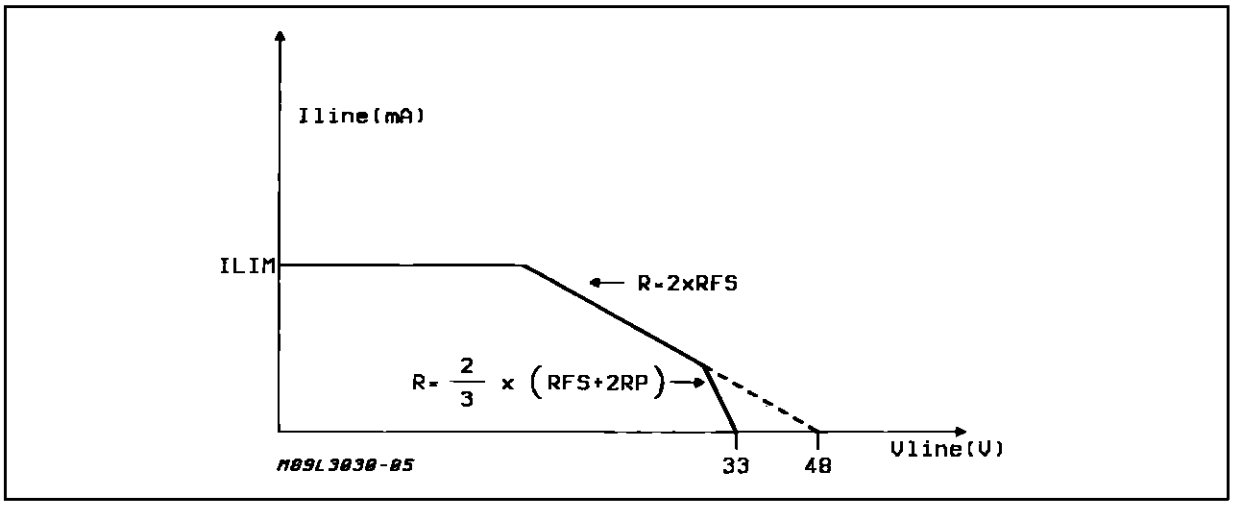
As far as the DC characteristic in Normal Battery is concerned, three different feeding conditions are present :

a) current limiting region ; the DC impedance of the SLIC is very high (> 20 Kohm) and therefore the system works like a current generator, the current value being set through the digital interface (25/30/45/70mA).
b) standard feeding system region ; the characteristic is equal to a – 48V (– 60V) battery (note 1), in series with two resistors, whose value is set by external components (see external component list of L3030).
c) low impedance region ; the battery value is reduced to 33V (45V) and the serial resistance is reduced to the value specified in stand by mode, that is : $\frac{2}{3} \times (RFS + 2RP)$

Switching between the three region is automatic without discontinuity, and depends on the loop resistance. Fig. 2 shows the DC characteristic in normal battery condition.

When the boost battery condition is activated the low impedance region can never be reached by the sy-

Figure 2 : DC Characteristic (n.b.) I_{LIM} = 25/30/45/70 mA.



Note : 1. This value of voltage battery, named apparent battery, is fixed internally by the control unit and is independent of the actual battery value. So, the voltage drop in the low impedance region is 15V. It is also possible to increase up to 25V this value setting BIT3R to 1.

stem ; in this case the internal dropout voltage is equal to 30V.

Fig. 3 shows the DC characteristic in boost battery condition.

In conversation mode, on request of control processor, whatever condition is set (normal or boost battery, direct or reverse polarity), you can inject the 12kHz (or 16kHz) signal (permanently applied at the pin 33 with 950mVrms typ. amplitude), as metering pulses. A patented automatic control system adjust the level of the metering signal, across the line, to 2Vrms setting BIT3 = 0, or to 5Vrms setting BIT3 = 1 ; this, regardless of the line impedance. Moreover the metering signal is ramped at the beginning and at the end of each pulse to prevent undesirable clicking noise ; the slope is determined by the value of CINT (see the external component list of L3030). The SLIC also provides, in the transmit direction (from line to 4-wire side), an amplifier to insert an external notch filter (series resonator) for suppressing the 12/16kHz residual signal.
Fig. 4 shows a suggested notch Filter configuration.

The metering pulses can be injected with a DC line current equal to zero (ON-HOOK Operation).

If teletax is not used the notch filter can be replaced by a 1KΩ resistor.

In conversation mode the AC impedance at the line terminals, ZML, is synthetized by the external components ZAC and RP, according to the following formula :

$$ZML = ZAC + (RP1 + RP2)$$

Depending on the characteristic of the ZAC network, ZML can be either a pure resistance or a complex impedance, so allowing ST SLIC to meet different standards as far as the return loss is concerned. The capacitor CCOMP guarantees stability to the system.

The two-to-four wire conversion is achieved by means of a Wheatstone bridge configuration, the sides of which being :

1) the line impedance (Zline),
2) the SLIC impedance at line terminals (ZML),
3) the network ZA connected between pin 36 and 41 of L3030 (see external component list of L3030),
4) the network ZB between pin 36 and ground that shall copy the line impedance.

For a perfect balancing, the following equation shall be verified :

$$\frac{ZA}{ZB} = \frac{ZML}{Zline}$$

It is important to underline that ZA and ZB are not obliged to be equal to ZML and to Zline, but they both may be multiplied by a factor (up to ten) so allowing use of smaller capacitors.

In conversation, the L3000S dissipates about 250mW for its own operation ; the dissipation depending on the current supplied to the line shall be added.

The fig 5 and fig 6 show the DC characteristic for two different Feeding resistance.
2 x 200 Ohm and 2 x 400 respectively.

Figure 3 : DC Characteristic (b.b.)
I_{LIM} = 25/30/45/70mA.

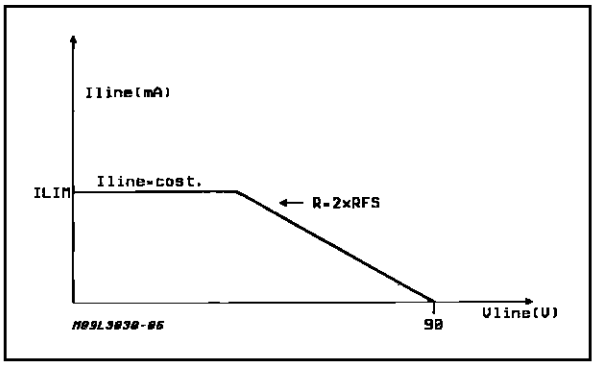
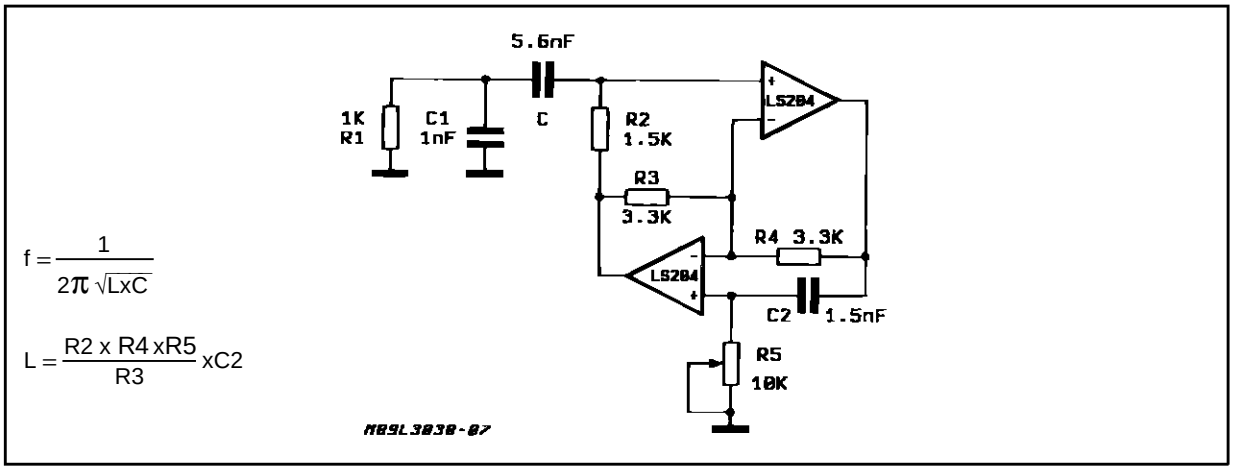


Figure 4 : External Teletaxe Filter.



$$f = \frac{1}{2\pi\sqrt{LxC}}$$

$$L = \frac{R2 \times R4 \times R5}{R3} \times C2$$

Figure 5 : DC Characteristic for 2 x 200 ohm Feeding System.

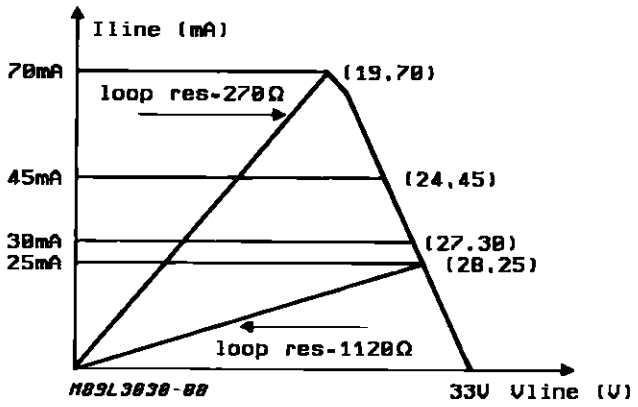


Figure 6 : DC Characteristic for 2 x 400 ohm Feeding System.

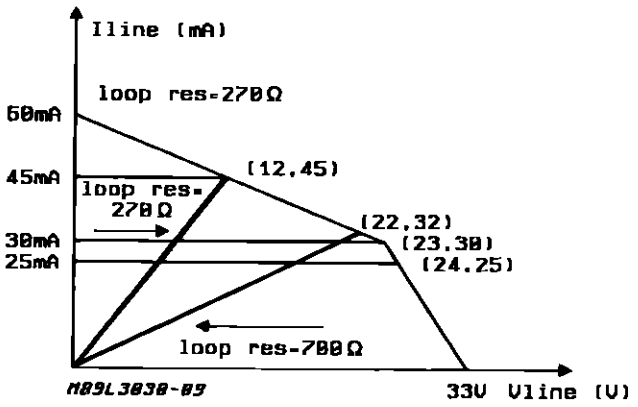
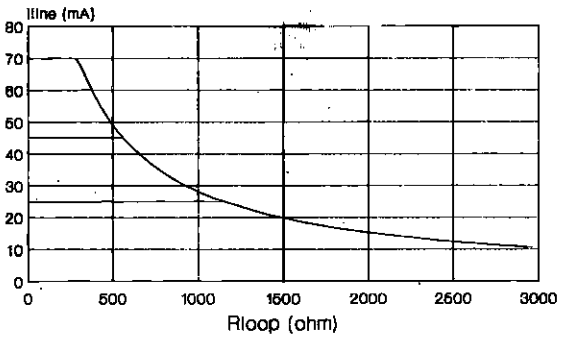


Figure 7 : Line Current Versus Loop Resistance, RFS = 200Ω, R_P = 30Ω, V_{B-} = –48V.



Ringing Mode

When ringing is selected (BIT2R = 1, BIT0R = 0), the control unit L3030 presets the L3000S to operate between – 48V (– 60V) and + 72V (+ 60V) battery. Then, setting BIT1 = 1, a low level signal (0.285Vrms with frequency range 16-66Hz) applied to pin 41, is amplified and injected in balanced mode to the line through L3000S with a superimposed DC voltage of 24V. The impedance to the line is given by the two external resistors and the 24V DC polarity can only be direct.

The first and the last ringing cycles are synchronized by L3030 so that ringing always starts and stops at zero crossing. Ring trip detection is performed autonomously by the SLIC, without any particular command, using a patented system ; when handset is lifted, SLIC suspends the ringing signal just remaining in the ringing mode. In this condition, the control unit L3030 checks that the loop is closed for a time equal to two periods of the ringing signal ; if the closure is confirmed, a flag (BIT0T = 1) is set and the SLIC waits the new command from the control processor. Whereas the loop closure is not confirmed, the ringing signal is newly applied to the line, without setting BIT0T.

DIGITAL INTERFACE

Functional Description

The L3030 states and functions are controlled by central processor through five wires defining a digital interface. It is possible to select the interface working mode between SERIAL or PARALLEL (pin 33 tied to a voltage between 4 and 5V).

1) Serial Mode

The five wires of the digital interface have the following functions :

- clock (DCLK), entering at pin 21
- data in/data out (DIO), exchanged at pin 20
- input/output select (EIA), entering at pin 18
- chip select (NCS), entering at pin 19
- change NCS from in to out (CI), entering at pin 26 (note 1)

The maximum clock frequency is 600Khz.

When EIA signal is low data are transferred from the card controller into I/O registers of the L3030 selected by NCS signal tied at low level ; then data are latched for execution. In this phase a complete 8 bit word is loaded into internal register and consequently NCS signal must remain low for the corresponding 8 clock pulses (DCLK). The EIA signal must remain at low level at least for the time in which NCS signal remain low. The device load data in input register during the positive edge of clock signal (DCLK) and store the contents of the register on the positive edge of NCS signal.

When EIA signal is high data are transferred from the L3030 selected by NCS tied to low level to the card controller. The L3030 status is described by five bits contained in the output register ; the NCS signal can remain low for five or less clock pulses depending if the card controller want to read the complete L3030 status or only a part of it.

Fig. 8, 9 show the complete write and read operation timing. Table 1 shows the meaning of each bit of an I/O data.

Table 1 : Serial Mode.

Meaning	Value			
Data in (note 2)				
BIT0R = Impedance (note 3)	0 - Stand-by/ringing			
	1 - Conversation			
BIT1R = TTX & Ring Timing (note 4)	0 - Timing off			
	1 - Timing on			
BIT2R = Ring (note 5)	0 - TTX Signal Injection			
	1 - Ring Signal Injection			
BIT3R = TTX Level	0 - Low Amplitude ($2V_{RMS}$)			
	1 - High Amplitude ($5V_{RMS}$)			
BIT4R = Battery Polarity	0 - Normal Polarity			
	1 - Reverse Polarity			
BIT5R = Extra Feeding	0 - Normal Battery			
	1 - Boosted Battery			
BIT6R Current Limiting BIT7R	0 25mA 0	0 30mA 1	1 45mA 1	1 70mA 0
Data Out (note 6)				
BIT0T = Line Supervision	0 - On Hook			
	1 - Off Hook			
BIT1T = Ground Key	1 - Long. Line Current < 17mA			
	0 - Long. Line Current > 17mA			
BIT2T = Internal Line Current Limiter (note7)	0 - Off			
	1 - On			
BIT3T = Line Voltage	0 - Normal			
	1 - Minus of Half Battery			
BIT4T = Thermal Overload (note 8)	1 - Off			
	0 - On			

Notes : 1. When CI signal is tied to low level, NCS signal is the chip select input ; with CI signal at high level, the NCS signal becomes an output that carry out the logical sum of the following bits : BIT0T, BIT1T.
2. The description of the commands is referred to the system L3030 + LINE INTERFACE module.
3. To set SBY mode with I_{lim} = 7mA : BIT0R = 0 and at least one of the two last bits (BIT6R ; BIT7R) must be set to 1.
4. TTX and RING signals are injected into the line interface module with BIT1R to "1".
5. To set RING mode at least one of the three last bits (BIT5R, BIT6R, BIT7R) must be set to 1, in addition BIT0R must be set to 0.
6. The description of the commands is referred to the system L3030 + LINE INTERFACE module.
7. The bit BIT2T is set to 1 when the SLIC is operating in Conversation Mode and into the limiting current region (short loop).
8. The bit BIT4T is set to 1 when the junction temperature of L3000S is about 140°C.

Figure 8 : Writing Operation Timing (serial mode).

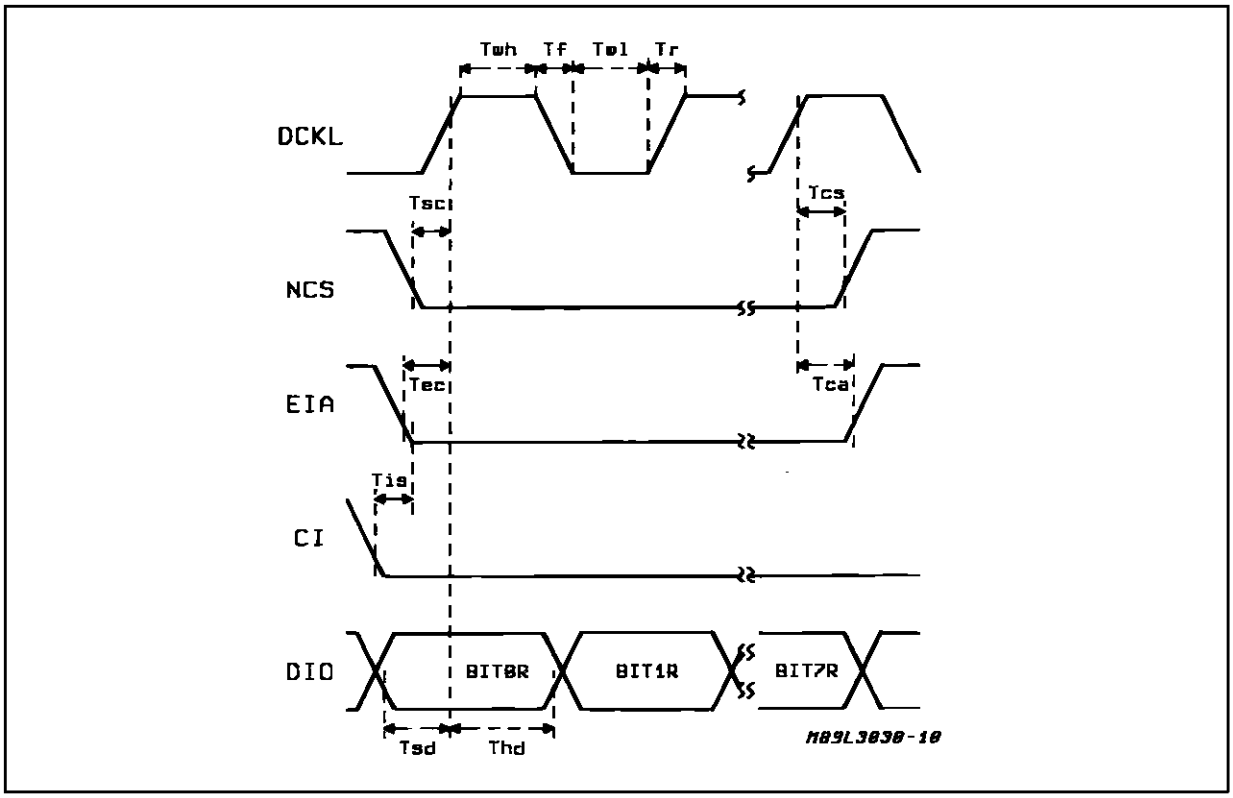
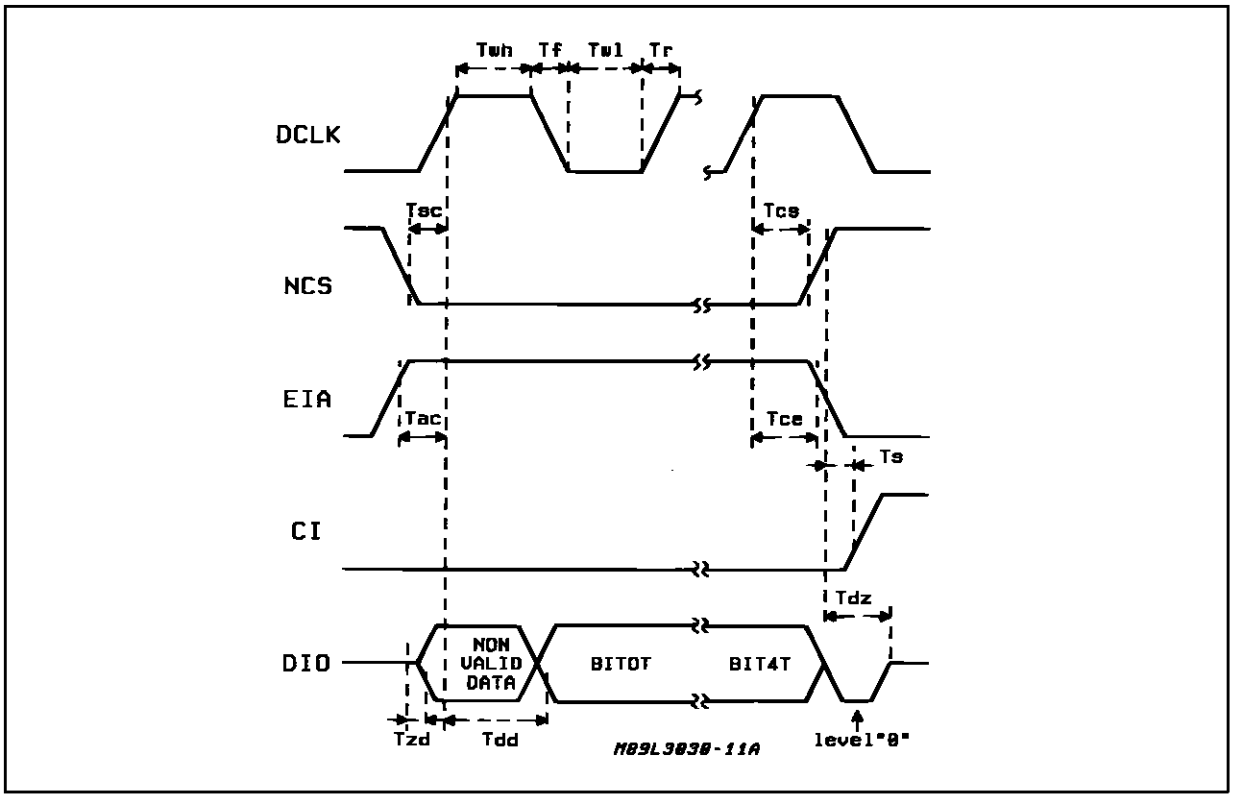


Figure 9 : Reading Operation Timing (serial mode).



2) Parallel Mode

This operating mode is enabled connecting pin 33 to a voltage in the range from 4V to 5V. The five wire have the following functions :
- power down/feeding (EIA), entering at pin 18
- timing (CI), entering at pin 26
- ring (DCLK), entering at pin 21
- on-hook/off-hook (NCS), outgoing at pin 19
- ground-key (DIO), outgoing at pin 20

In this operating mode the signals at the inputs are immediately executed, without any external clock timing ; all the internal registers are bypassed. The informations sent back on pins 19 and 20, display in real time the setting of internal circuits, that means line status. In the table 2 the correspondence between the interface wires in the parallel mode and equivalent bit in serial mode is pointed out ; where there isn't this correspondence, the internal setting is shown.

Table 2 : Parallel Mode.

Pin	Rif.	Meaning (note 1)	Eq. Bit of Ser. Interf.	Value
18	EIA	PD/feeding	BIT0R	0 : High Impedance
				1 : Low Impedance
26	CI	Timing	BIT1R	0 : Ring Timing Off
				1 : Ring Timing On
21	DCKL	Ring	BIT2R	0 : No Ring
				1 : Ring Injection
			BIT3R	0 : Low Amplitude
			BIT4R	0 : Normal Polarity
			BIT5R	0 : Normal Battery
			BIT6R	0 :
			BIT7R	1 : Line Curr. = 30mA
19	NCS	On-hook/off-hook	BIT0T	0 : On-hook
				1 : Off-hook
20	DIO	Ground Key	BIT1T	1 : Long. Curr. < 17mA
				0 : Long. Curr. > 17mA
			BIT2T	
			BIT3T	
			BIT4T	

Note : 1. The description of the commands is referred to the system L3030 + LINE INTERFACE module.

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS

(V_{DD} = + 5V, V_{SS} = – 5V, $T_{amb.}$ = 25°C) (refer to PLCC44 package)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
STATIC ELECTRICAL CHARACTERISTICS						
Vil	Input Voltage at Logical "0"	Pins 18, 19, 20, 21, 26	0		0.8	V
Vih	Input Voltage at Logical "1"		2.0		5	V
Iil	Input Current at Logical "0"	Vil = 0V			200	µA
Iih	Input Current at Logical "1"	Vih = 5V			10	µA
Vol	Output Voltage at Logical "0"	Pins 19, 20 Iout = – 1mA			0.4	V
Voh	Output Voltage at Logical "1"	Pins 19, 20 Iout = 1mA	2.4			V
Ilk	Tristate Leak. Current	Pin 20 NCS = "1"			10	µA

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC ELECTRICAL CHARACTERISTICS						
fclk	Clock Frequency		1		600	kHz
Tr, Tf	Clock Rise and Fall Time				50	ns
Twh, Twl	Clock Impulse Width		750			ns
Tis	CI to NCS Set up Time		300			ns
Tec	”0” EIA to DCKL Set up Time		300			ns
Tsc	DCKL to NCS Delay (+ edge)		300			ns
Tsd	Data in Set up Time		0			ns
Thd	Data in Hold Time		800			ns
Tcs	NCS to DCKL Hold Time		800			ns
Tca	”0” EIA to DCKL Hold Time		900			ns
Tac	”1” EIA to DCKL Set up Time		400			ns
Tzd	Data out to ”0” NCS Delay		0		600	ns
Tce	”1” EIA to DCKL Hold Time		900			ns
Tdz	Data out to ”1” NCS Delay				500	ns
Tdd	Data out to DCKL Delay				1500	ns
Tsi	”0” CI to NCS Hold Time		300			ns

OPERATION DESCRIPTION

To set SLIC in operation the following parameters have to be defined :

- the DC feeding resistance RFS, defined as the resistance of each side of the traditional feeding system (most common values are 200, 400 or 500 ohm).
- the AC impedance at line terminals, ZML, to which the return loss measurement references. It can be real (typically 600 ohm) or complex.
- the equivalent AC impedance of the line Zline, when evaluating the trans hybrid loss (2/4 wire conversion). It is usually a complex impedance.
- the ringing signal frequency Fr (ST SLIC allows frequency ranging from 16 to 66Hz).
- the metering pulse frequency Ft (two values are possible : 12kHz or 16kHz).
- the value of the two resistors RP1/RP2 in series with the line terminals ; main purpose of the a.m. resistors is to allow primary protection to fire. ST suggest the minimum value of 50 ohm for each side.

On this assumptions, the following component list is defined.

EXTERNAL COMPONENT LIST FOR THE LINE INTERFACE

Pin	Component		Involved Parameter or Function
	Ref.	Value	
L3000S			
10	RREF	24.9kΩ ± 1%	Bias Resistance
1,15	RP	30 to 100Ω	Line Series Resistor
7	CDVB	47µF – 20V	Battery Voltage Rejection
3	CVB+	0.1µF – 100V (1)	Positive Battery Filter
8	CVB–	0.1µF – 100V (2)	Negative Battery Filter
8	D1	BAT 49X	Protective Shottky Diode
L3030 (PLCC44)			
4-3	CVSS	0.1µF – 15V	Negative Supply Voltage Filter
5-3	CVDD	0.1µF – 15V	Positive Supply Voltage Filter
7-8	RR	16KΩ (range: 10 to 50KΩ)	Capacitor Multiplier Gain (8)
15-17	RDC	2 x (RFS – RP1)	DC Feeding Resistor (RDC > 270Ω)
7-15	CAC1 (3)	$\frac{1}{6.28 \times 250 \times (ZAC + RDC)}$	AC Path decoupling
14-15	CAC2	CAC1	
8-9	ZAC	ZML – (RP1 + RP2)	2 Wire AC impedance
8-9	CCOMP	1/(6.28 x 150000 x (RPC))	AC loop compensation
9-14	RPC	RP1 + RP2	Rp insertion loss compensation
2-3	RREF	24.9KΩ 1%	Bias Resistance
36-3	ZB	K x Zline (note 4)	Line Impedance Balancing Network
36-41	ZL	K x RPC in Series with K x ZAC // (CCOMP/K)	SLIC Impedance Balancing Network (note 5)
32-3	CINT	(note 6)	Ring trip detection time constant
15-16	Ccon	0.15µF (note 7)	Interface Time Constant
35	TTx FILT.	Z_{TTX} = 1kΩ 1% in speech band $Z_{TTX} \approx 0\Omega$ at TTX freq. (note 9)	Teletax filter.
34	R_{GTTX}	10kΩ 1%	Teletax filter.

Notes :

1. In case line cards with less than 7 subscribers are implemented CVB– capacitor should be equal to 680nF/N where N is the number of subscriber per card.
2. This shottky diode or equivalent is necessary to avoid to damage to the device during hot insertion or in all those cases when a proper power up sequence cannot be guaranteed.
   In case the shottky diode is not implemented the power sequence should guarantee that VB+ is always the last supply applied at power on and the first removed at power off.
   In case an other shottky diode type is adopted it must fulfill the following characteristics:
   V_F < 450mV @ I_F = n · 15mA, T_{amb} = 25°C
   V_F < 350mV @ I_F = n · 15mA, T_{amb} = 50°C (T_{jL3000} = 90°C)
   V_F < 245mV @ I_F = n · 15mA, T_{amb} = 85°C (T_{jL3000} = 120°C)
   Where n is the number of line sharing the same diode.
3. If the internal capacity multiplier stage is not used, pin 7 must be connected with pin 14 without mounting RR and CAC2. In this case CAC1 = 1/(6.28 x 30 x RDC).
4. The structure of this network shall copy the line impedance, in case multiplied by a factor K = 1....10
5. K as fixed at note 4.
6. CINT can have the following values :

Fr. (Hz)	16/18	18/21	21/26	26/31	31/38	38/46	46/57	57/66
CINT (nF)	560	470	390	330	270	220	180	150

7. Ccon is necessary to work "without on/off hook detection-errors" during TTX-pulses.
8. RR is used by a capacitor multiplier circuit to synthetize an higher AC/DC splitting capacitor starting from CAC1 and CAC2. Supposing CAC1 = CAC2 = CAC the synthetized capacitor value will be equal $\frac{RR + ZML}{ZML} \cdot CAC$.
9. If Teletax is not used the TTX FILT. can be replaced by a 1kΩ resistor.

Figure 10 : Typical Application Schematic Diagram.

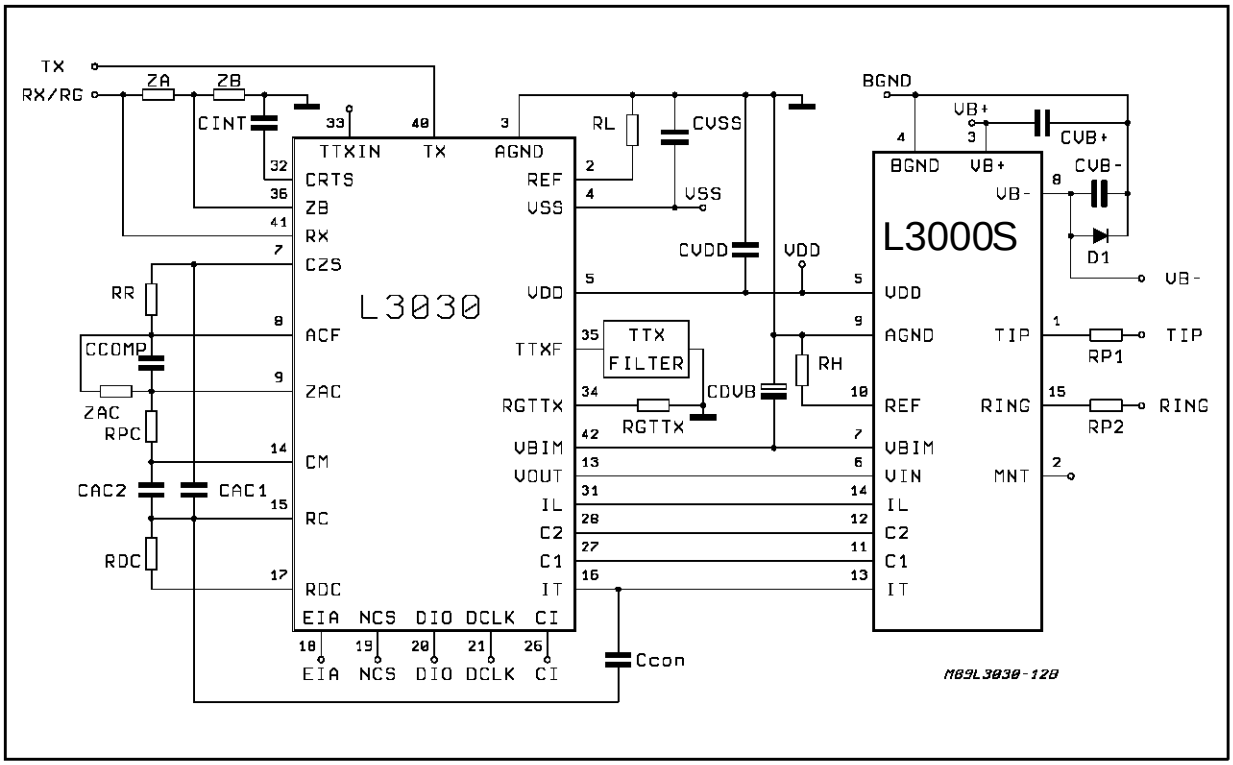
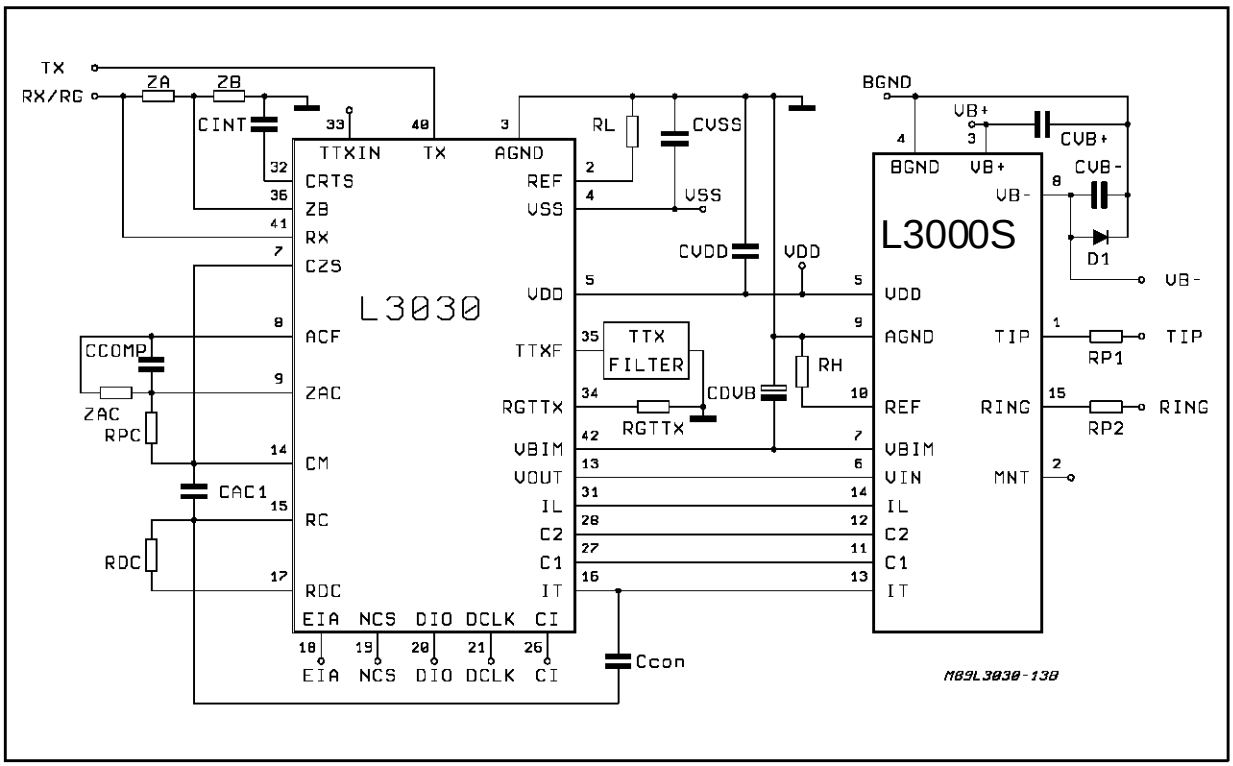


Figure 11 : Typical Application Schematic Diagram without Capacitor Multiplier.



ELECTRICAL CHARACTERISTICS (refer to the test circuits of the Figure 12, V_{DD} = + 5V, V_{SS} = - 5V, V_B+ = + 72V, V_B– = – 48V, T_{amb} = + 25°C, TTX FILT = 1kΩ)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
STAND-BY						
Vls	Output Voltage at L3000S Terminals	Iline = 0mA Iline = 5mA	30.0 28.2		40.0 38.5	V V
Ilcc	Short Circuit Current	DATA IN (note 1) 000X00X1	5		8.5	mA
Iot	On/off-hook Detection Threshold		5		8.5	mA
Vls	Symmetry to Ground	Iline = 0mA			.75	V
STAND BY DENIAL						
Ilcc	Short Circuit Current	DATA IN 000X00X0			2	mA
DC OPERATION - NORMAL BATTERY (V_{TTX} = 2V_{RMS}, low level)						
Vlo	Output Voltage at L3000S Terminals Ilim = 70mA Data in 1000X010	Iline = 0mA Iline = 20mA Iline = 50mA	31.0 24.0 2.5		35.0 28.8 17.5	V V V
Ilim	Current Programmed Through the Digital Inter.		– 10%	Ilim	+ 15%	mA
Io	On-hook Detection Threshold				8	mA
If	Off-hook Detection Threshold		12			mA
Ilgk	Longitudinal Line Current with GK Detect		10	17	26	mA
DC OPERATION - BOOST BATTERY						
Vlo	Output Voltage at L3000S Terminals	Iline = 0mA Iline = 20mA	86 68.6		95.6 81	V V
AC OPERATION						
Ztx	Sending Output Impedance 4 Wire Side				10	Ω
Zrx	Receiving Input Impedance 4 Wire Side		100			kΩ
THD	Signal Distorsion at 2W and 4W Terminals				0.5	%
R1	2W Return Loss	f = 300 to 3400Hz	22			dB
Thl	Trans Hybrid Loss	f = 300 to 3400Hz	24			dB
Gs	Sending Gain	Vso = 0dBm f = 1020Hz Norm. Polarity	– 0.25		+ 0.25	dB
Gsf	Sending Gain Flatness versus Frequency	f = 300 to 3400Hz Respect to 1020Hz	– 0.1		+ 0.1	dB
Gsl	Sending Gain Linearity	fr = 1020Hz, Vsoref = –10dBm Vso = + 4 /– 40dBm	– 0.1		+ 0.1	dB
Gr	Receiving Gain	Vri = 0dBm f = 1020Hz Norm. Polarity	– 0.25	0	+ 0.25	dB
Grf	Receiving Gain Flatness	f = 300 to 3400Hz Respect to 1020	– 0.1		+ 0.1	dB

Notes : 1. The data into the digital interface of L3030 are send in serial mode. The format of data is the following :
a) DATA IN : the bit at left side is BIT 0 of the writing word, while the bit at the right side is BIT 7.
b) DATA OUT : the bit at the left side is BIT0 of the reading word, while the bit at the right is BIT4.
When appear a symbol X, the value of the bit don't care.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AC OPERATION (continued)						
Grl	Receiving Gain Linearity	fr = 1020Hz, Vriref = – 10dBm Vri = + 4 /– 40dBm	– 0.1		+ 0.1	dB
Np4W	Psophometric Noise at 4W-Tx Terminals			– 75	– 70	dBmp
Np2W	Psophometric Noise at Line Terminals			– 75	– 70	dBmp
SVRR	Supply Voltage Rejection Ratio Relative to VB–	f = 3400Hz			– 30	dB
SVRR	Relative to V_{DD}	f = 3400Hz Vs = 100mVrms		– 30	– 26	dB
SVRR	Relative to V_{SS}			– 32	– 30	dB
Ltc	Longitudinal to Transversal Conversion	f = 300 to 3400Hz Iline = 30mA, ZML = 600Ω	49 (1)	60		dB
Tlc	Transversal to Longitudinal Conversion		48	51		dB
Td	Propagation Time	Both Direction			40	µs
Tdd	Propag. Time Distortion				25	µs
Vttx	Line Voltage of Teletaxe Signal	V_{TTXin} = 950mVrms Note 2 Note 3	1.7 4.5		2.3 5.5	V V
THD	Teletaxe Signal Harmonic	Dist. ttx Filt = 0Ω @ 16kHz Note 4			5	%
Zitt	Teletaxe Amplif. Input Impedance	Pin 33 of L3030	100			kΩ
AC OPERATION BOOST BATTERY						
Gs	Sending Gain	Vso = 0dBm f = 1020Hz Norm. Polarity	– 0.66	– 0.16	+ 0.34	dB
Gr	Receiving Gain	Vri = 0dBm f = 1020Hz Norm. Polarity	– 0.27	+ 0.08	+ 0.43	dB
Np4W	Psophometric Noise at 4W-Tx Terminals			– 73	– 68	dBmp
Np2W	Psophometric Noise at line Terminals			– 73	– 68	dB
SVRR	Relative to Vdd	f = 3400Hz Vs = 100mVrms			– 23	dB
SVRR	Relative to Vss				– 23	dB
RINGING PHASE						
Vlr	Superimposed DC Voltage	Rloop > 100kΩ Rloop = 1kΩ	19 17	23 21	27 25	V V
Vacr	Ringing Signal at Line Termin.	Rloop = 1kΩ/1µF	56			Vrms
If	DC Off-hook Det. Threshold		1.5		3.5	mA
Ilim	Current Limit.		85		130	mA
Vrs	Ringing Simmetry				2	Vrms
THDr	Ringing Signal Distortion	V_{AC} = 0.285V_{RMS} f_{RING} = 30Hz			5	%

Notes : 1. Up to 52dB using selected L3000S.
2. The configuration of data sent to device change, every 100mS, from - 1100X010 - to - 1000X010 -
3. The configuration of data sent to device change, every 100mS, from - 1101X010 - to - 1001X010 -
4. Error generated by ttx filt ≠ 0 ohm, on the output teletax amplitude is err% = 100 x (1 + A) x B/C where A = 10 Kohm/RGTTX[Kohm], B = TTXFILT[Kohm], C = (TTXFILT[Kohm] + 1 Kohm), for example 10 ohm means err% = 2%.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
RINGING PHASE						
Zir	Ringing Amplif. Input Impedance	Pin 41 of L3030	100			kΩ
Vrr	Residual of Ringing Signal at TX Output				600	mV
Trt	Ring Trip Detection Time	fring = 16Hz T = 1/fring	(1T)		125 (2T)	ms
Toh	Off-hook Status Delay after the Ringing Stop				125 (2T)	ms
Trs	Cut off of Ringing	Ring Trip not Confirmed			188 (3T)	ms
SUPPLY CURRENT						
IDD	Positive Supply Current CS = 1	Stand-by Conversation (NB/BB) Ringing		16.0 26.0 16.5	20.0 31.0 21.0	mA mA mA
ISS	Negative Supply Current CS = 1	Stand-by Conversation (NB/BB) Ringing		9 19 9	12 23 12	mA mA mA
I_{BAT-}	Negative Battery Supply Current Line Current = 0mA	Stand-by Conversation NB Conversation BB Ringing		2 5 6.6 14	2.5 6.5 8.0 17	mA mA mA mA
I_{BAT+}	Positive Battery Supply Current Line Current = 0mA	Stand by Conversation NB Conversation BB Ringing		10 10 8 12	15 15 10 13.5	µA µA mA mA

NB = Normal Battery
BB = Boosted Battery

Figure 12 : Slic Test Circuit Schematic.

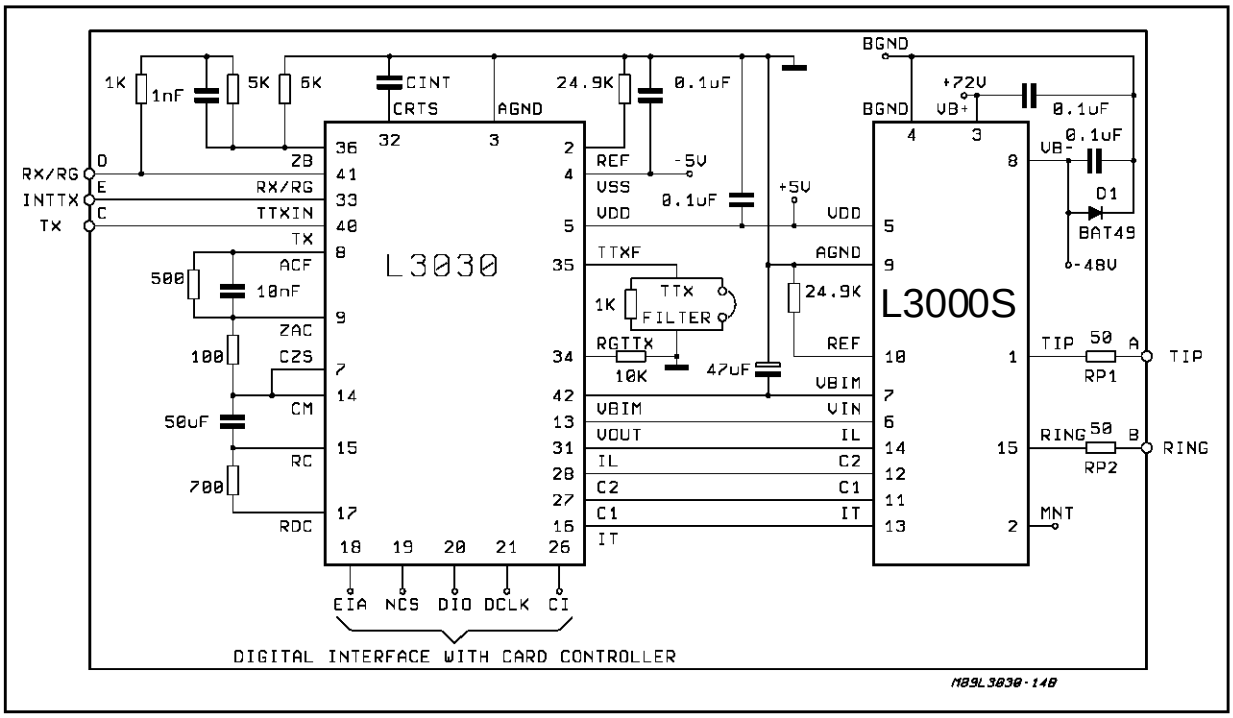


Figure 13: Typical application schematic with 2nd generation COMBO.

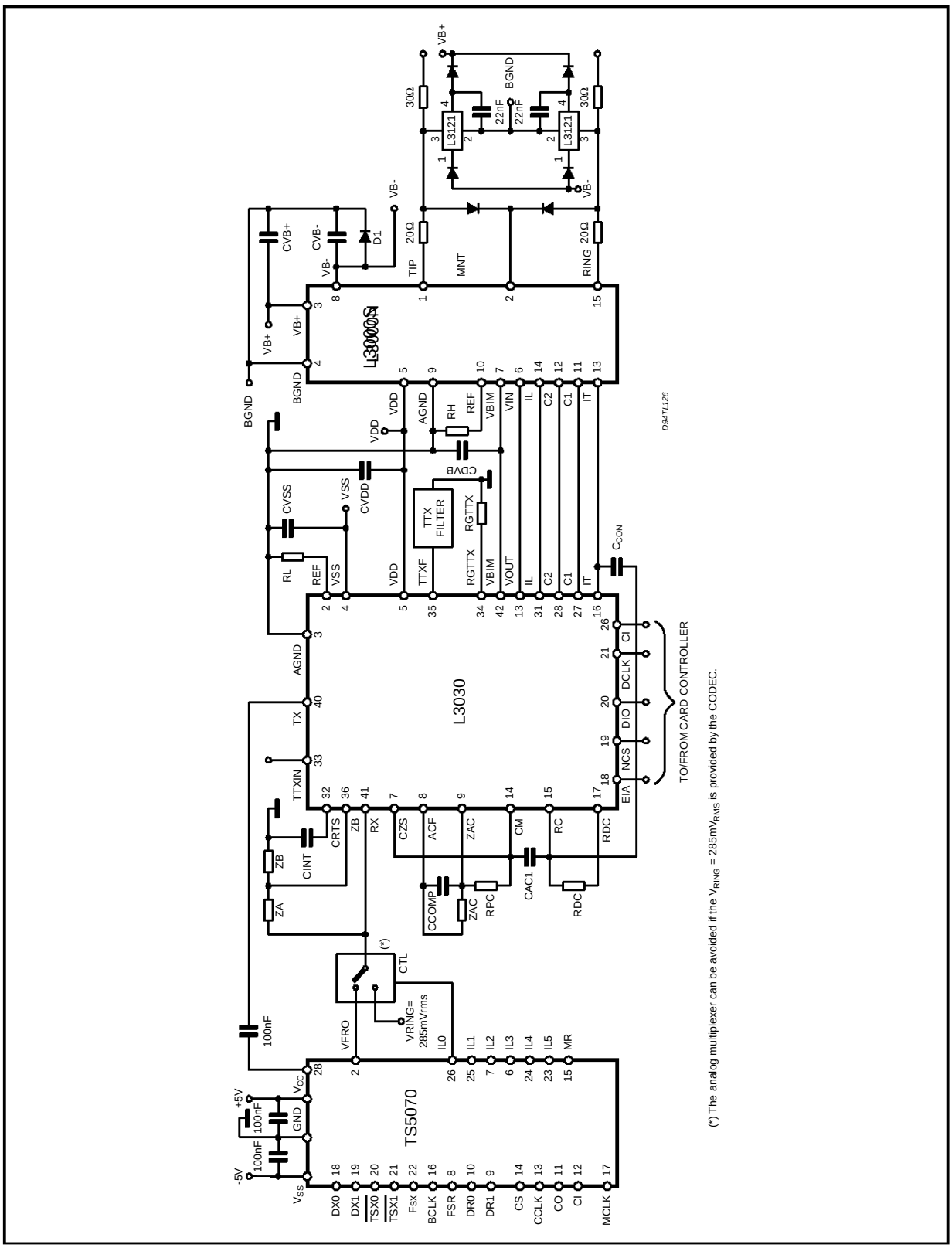
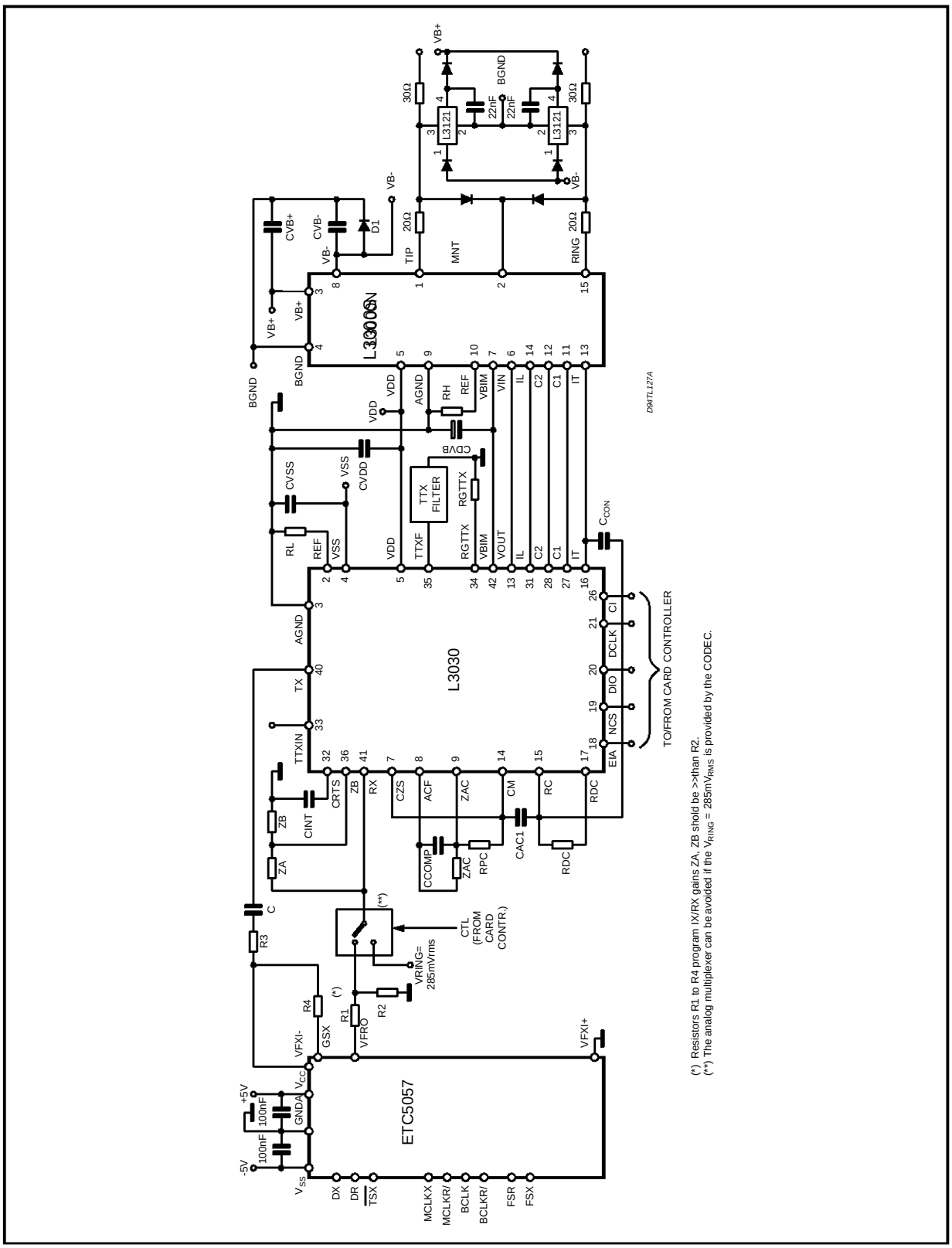


Figure 14: Typical application schematic with 1st generation COMBO.



APPENDIX

SLIC TEST CIRCUITS

Referring to the test circuit reported at the end of each SLIC data sheet here below you can find the proper configuration for each measurement.

In particular : A-B : Line terminals

C : TX sending output on 4W side

D : RX receiving input on 4W side

E : TTX teletaxe signal input

R_{GIN} : low level ringing signal input.

TEST CIRCUITS

Figure 1 : Symmetry to Ground.

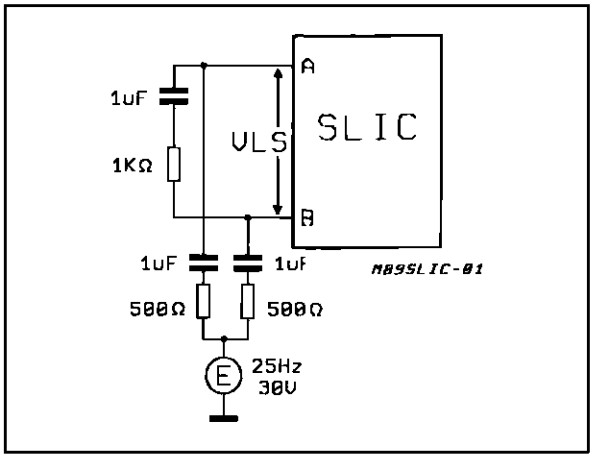
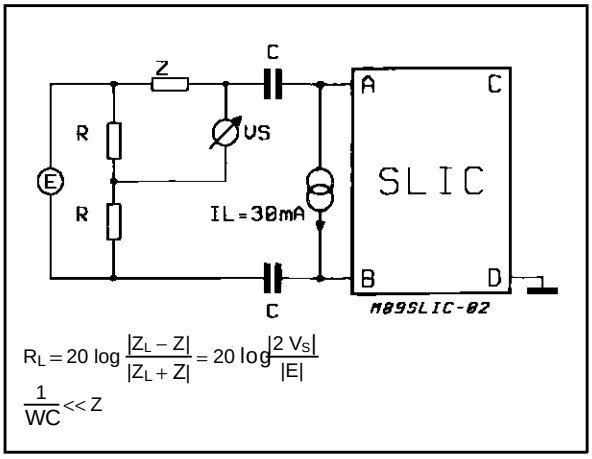


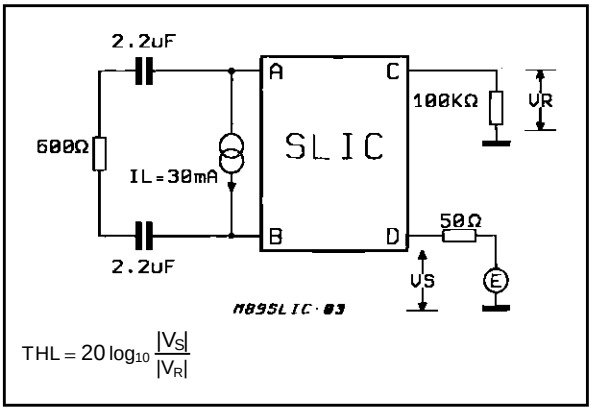
Figure 2 : 2W Return Loss.



$$R_L = 20 \log \frac{|Z_L - Z|}{|Z_L + Z|} = 20 \log \frac{|2\ V_S|}{|E|}$$

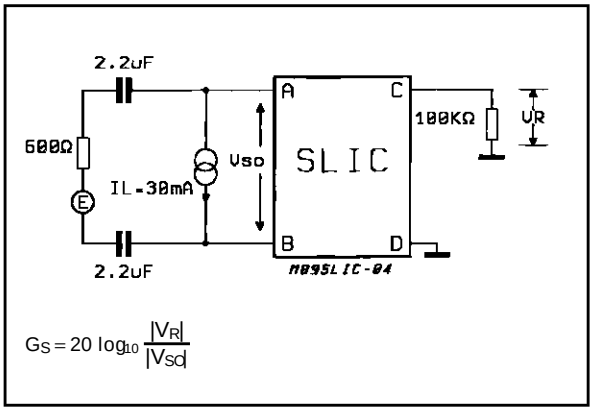
$$\frac{1}{WC} << Z$$

Figure 3 : Trans-hybrid Loss.



$$THL = 20 \log_{10} \frac{|V_S|}{|V_R|}$$

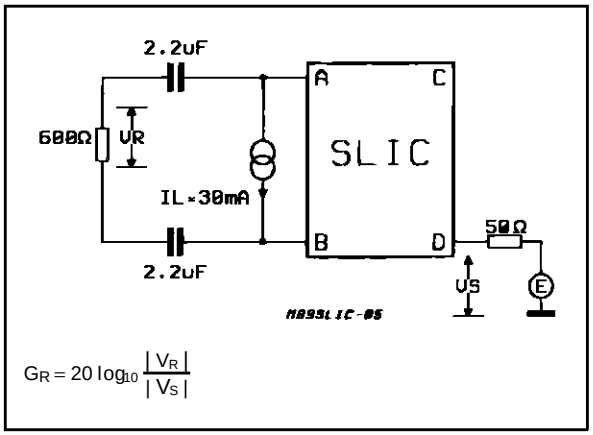
Figure 4 : Sending Gain.



$$G_S = 20 \log_{10} \frac{|V_R|}{|V_{SO}|}$$

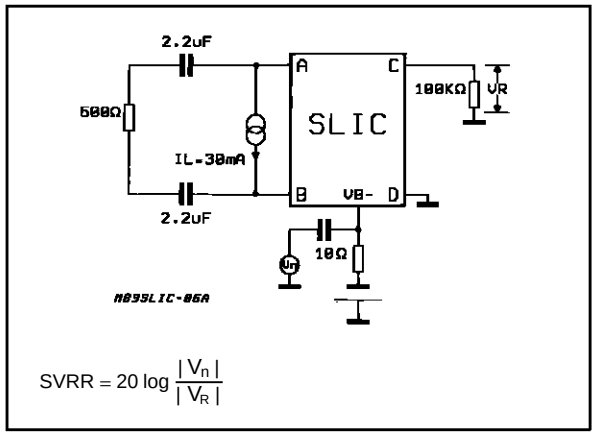
TEST CIRCUITS (continued)

Figure 5 : Receiving Gain.



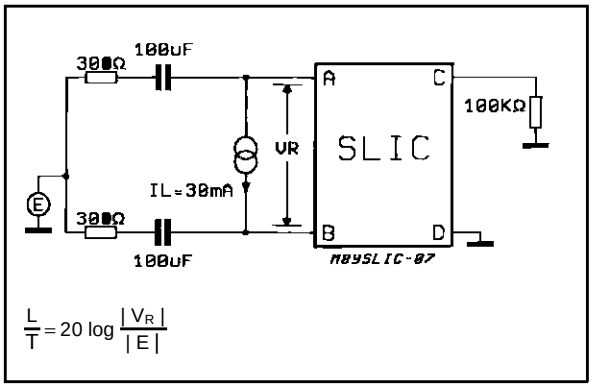
$$G_R = 20 \log_{10} \frac{|V_R|}{|V_S|}$$

Figure 6 : SVRR Relative to Battery Voltage VB–.



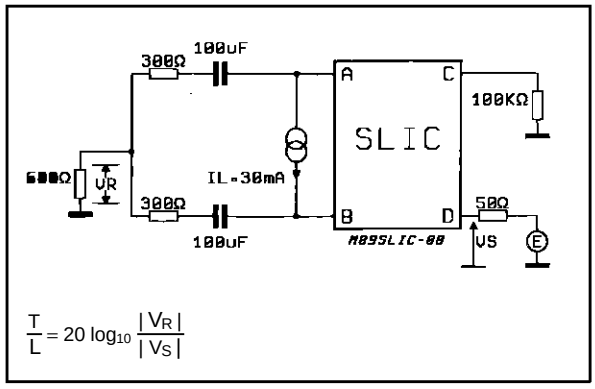
$$SVRR = 20 \log \frac{|V_n|}{|V_R|}$$

Figure 7 : Longitudinal to Transversal Conversion.



$$\frac{L}{T} = 20 \log \frac{|V_R|}{|E|}$$

Figure 8 : Transversal to Longitudinal Conversion.



$$\frac{T}{L} = 20 \log_{10} \frac{|V_R|}{|V_S|}$$

Figure 9 : TTX Level at Line Terminals.

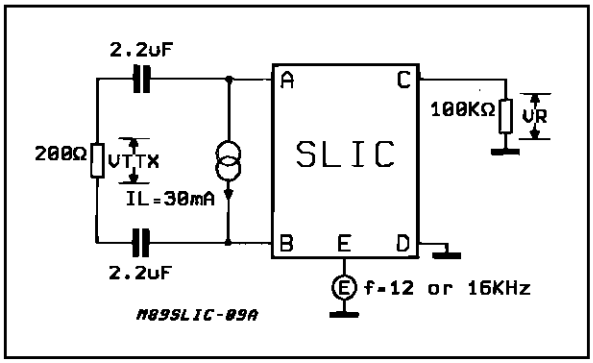
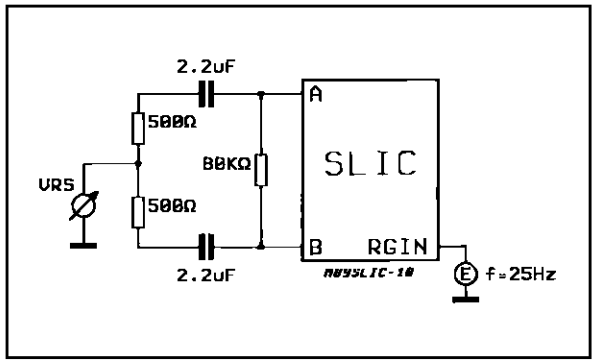
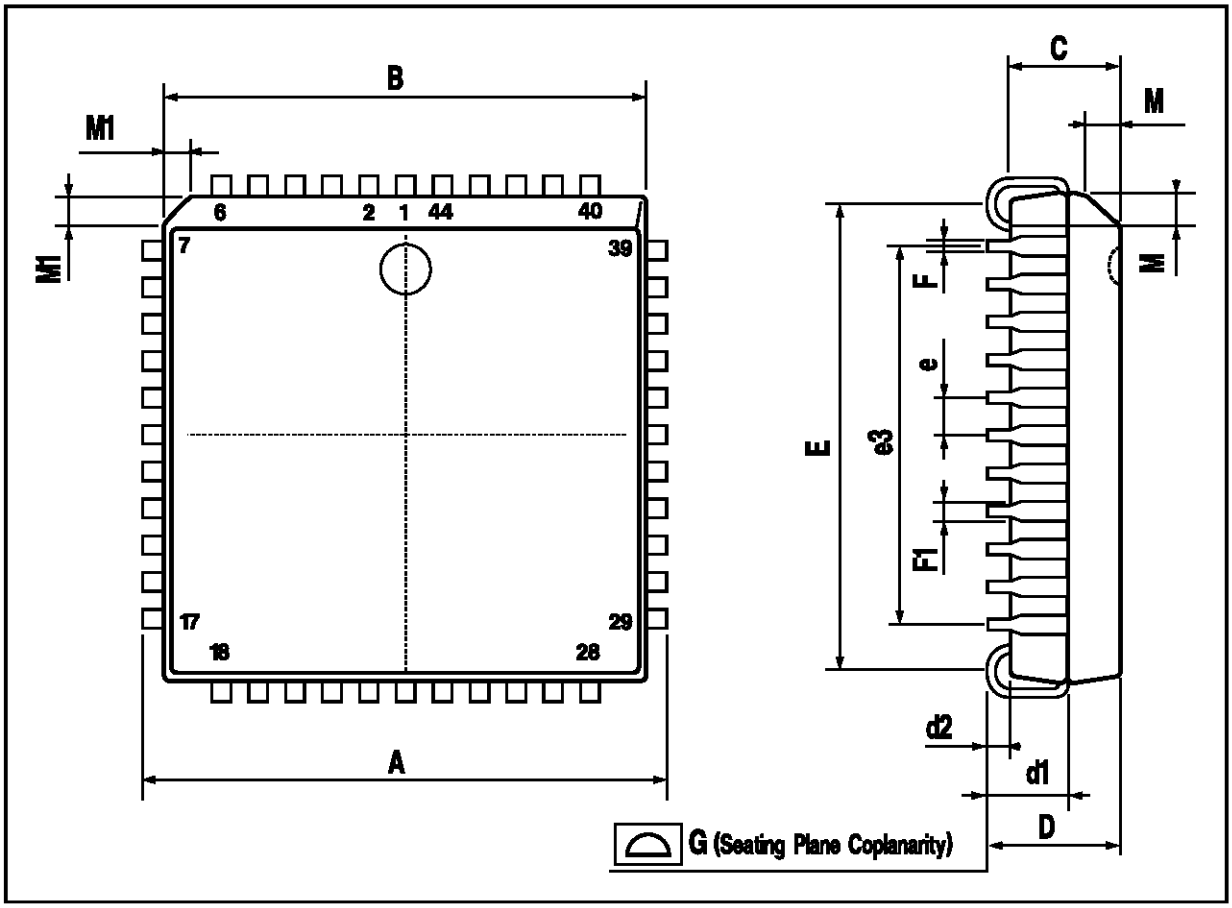


Figure 10 : Ringing Simmetry.



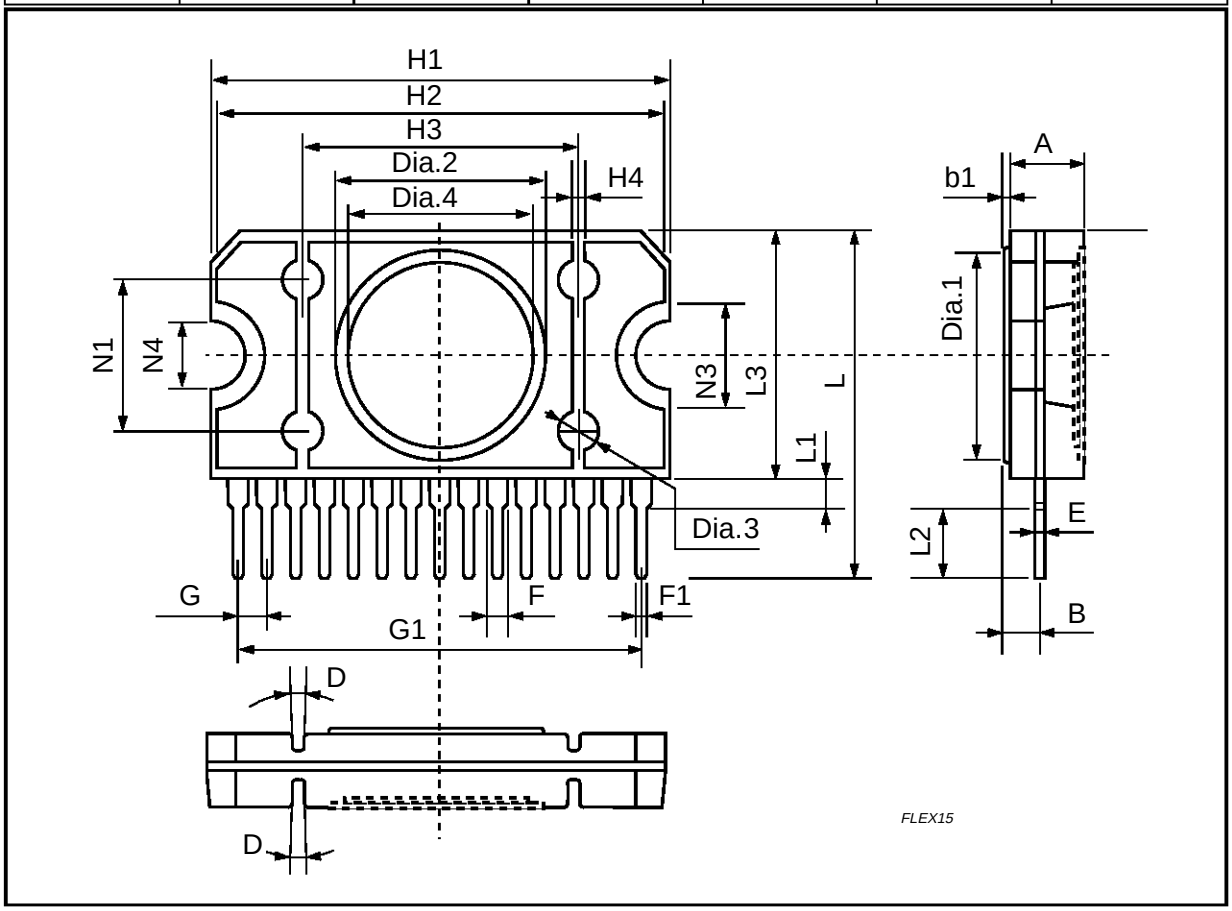
PLCC44 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	



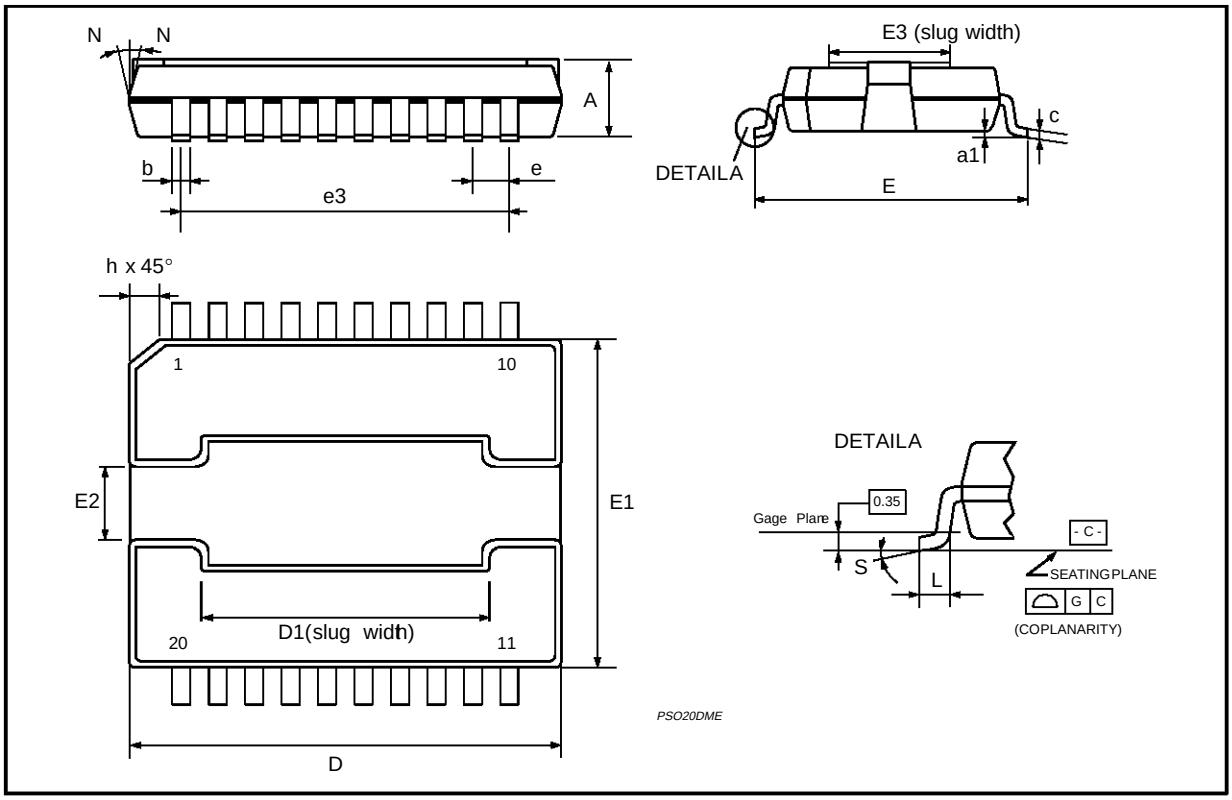
FLEXIWATT 15 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5.00			0.196
B			1.90			0.074
b1			0.1			0.004
D		4° (typ.)				
E		0.30			0.012	
F		0.90			0.035	
F1			0.57			0.022
G	1.77	1.9	2.03	0.070	0.075	0.080
G1		26.77			1.054	
H1		29.00			1.142	
H2		28.00			1.102	
H3		17.00			0.669	
H4		0.80			0.031	
L	19.05		19.95	0.75		0.785
L1	1.10		1.40	0.043		0.055
L2	2.60		2.90	0.102		0.114
L3	15.35		15.65	0.604		0.616
N1		10			0.394	
N3		6.8			0.268	
N4		3.8			0.15	
Dia1		13.00			0.511	



PowerSO-20 (slug-up) PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.70			0.145
a1	0		0.25	0		0.01
b	0.40		0.53	0.016		0.021
c	0.23		0.32	0.009		0.012
D	15.80		16.00	0.622		0.63
D1	9.4		9.80	0.37		0.385
E	13.90		14.50	0.547		0.57
e		1.27			0.05	
e3		11.43			0.45	
E1	10.90		11.10	0.429		0.437
E2			2.90			0.114
E3	5.80		6.20	0.228		0.244
G	0		0.10	0		0.004
h			1.10			0.043
L	0.80		1.10	0.031		0.043
N	10° (Max.)					
S	8° (Max.)					



PowerSO20 (slug-down) PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10	0		0.0039
b	0.40		0.53	0.0157		0.0209
c	0.23		0.32	0.009		0.0126
D (1)	15.80		16.00	0.6220		0.6299
E	13.90		14.50	0.5472		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.90		11.10	0.4291		0.437
E2			2.90			0.1141
G	0		0.10	0		0.0039
h			1.10			
L	0.80		1.10	0.0314		0.0433
N	10° (max.)					
S	8° (max.)					
T		10.0			0.3937	

(1) "D and E1" do not include mold flash or protrusions
- Mold flash or protrusions shall not exceed 0.15mm (0.006")