

Am25L02/25L03/25L04

Low-Power, Eight-Bit/Twelve-Bit Successive Approximation Registers

Distinctive Characteristics

- Contains all the storage and control for successive approximation A-to-D converters.
- Can be operated in START-STOP or continuous conversion mode.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Can be used as serial-to-parallel converter or ring counters.

FUNCTIONAL DESCRIPTION

The Am25L02, Am25L03 and Am25L04 are 8-bit and 12-bit TTL Successive Approximation Registers. The registers contain all the digital control and storage necessary for successive approximation analog-to-digital conversion. They can also be used in digital systems as the control and storage element in recursive digital routines.

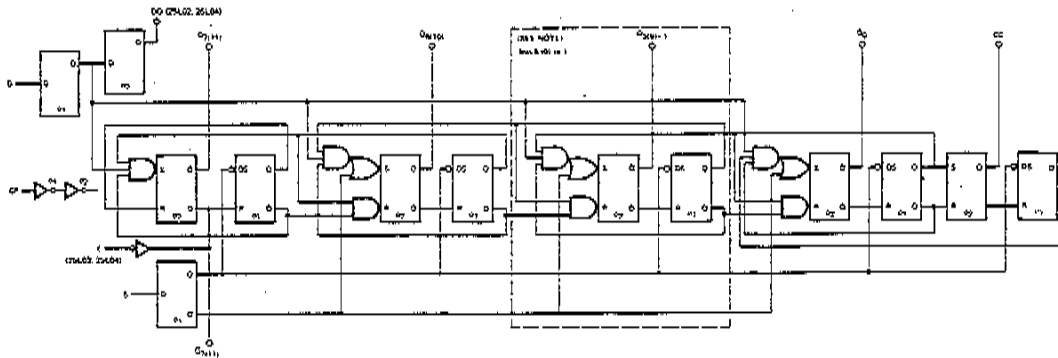
The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the Am25L02 and Am25L04 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration.

The register is reset by holding the \bar{S} (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state Q₇(11) LOW, (Note 2) and all the remaining register outputs HIGH. The $\bar{C}\bar{C}$ (Conversion Complete) signal is also set HIGH at this time. The \bar{S} signal should not be brought back HIGH until after the clock LOW-to-HIGH transition in order to guarantee correct resetting.

After the clock has gone HIGH resetting the register, the \bar{S} signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the Q₇(11) register bit and the Q₆(10) register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the Q₆(10) register bit and Q₅(9) is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q₀, the $\bar{C}\bar{C}$ signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

In order to allow complementary conversion the complementary output of the most significant register bit is made available. An active LOW enable input, \bar{E} , on the Am25L03 and Am25L04 allows devices to be connected together to form a longer register by connecting the clock, D, and \bar{S} inputs together and connecting the $\bar{C}\bar{C}$ output of one device to the \bar{E} input of the next less significant device. When the Start signal resets the register, the \bar{E} signal goes HIGH, forcing the Q₇(11) bit HIGH and inhibiting the device from accepting data until the previous device is full and its $\bar{C}\bar{C}$ goes LOW. If only one device is used the \bar{E} input should be held at a LOW logic level (Ground). For continuous conversion the $\bar{C}\bar{C}$ output is connected to the \bar{S} input so that the device automatically restarts at the end of a conversion. If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the $\bar{C}\bar{C}$ signal to indicate the end of conversion.

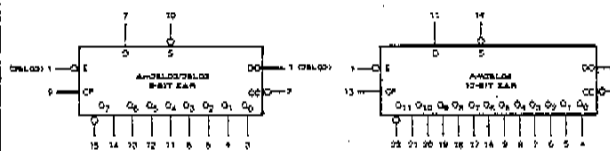
LOGIC DIAGRAMS



Notes: 1. Cell logic is repeated for register stages. Q₅ to Q₁ Am25L02/3, Q₉ to Q₁ Am25L04.
 2. Numbers in parentheses are for Am25L04.

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LOGIC SYMBOLS



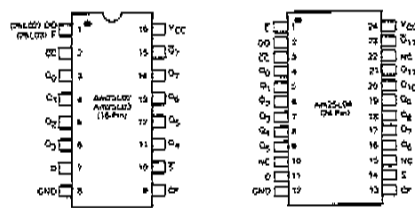
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V_{CC} = Pin 16
 GND = Pin 8

V_{CC} = Pin 24
 GND = Pin 12
 NC = Pins 10, 15, 22

CONNECTION DIAGRAMS Top Views



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Note: Pin 1 is marked for orientation.

LIC-238

MAXII
 Storage
 Tempera
 Supply V
 DC Volt
 DC Inpu
 Output (C
 DC Inpu

ELECT
 Am25L0
 Am25L0
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 V_{OH}
 V_{OL}
 V_{IH}
 V_{IL}
 I_{IL}
 I_{IH}
 I_{SC}
 I_{CC}

Notes: 1.
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 t_{pd+}
 t_{pd+}
 t_{pd-}
 t_{s(D)}
 t_{s(S)}
 t_{pd+}
 t_{pd-}
 t_{pwL}
 t_{pwH}
 t_{max}

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	
Temperature (Ambient) Under Bias	-65°C to +150°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	-55°C to +125°C
DC Voltage Applied to Outputs for High Output State	-0.5V to +7V
DC Input Voltage	-0.5V to +V _{CC} max.
Output Current, Into Outputs	-0.5V to +5.5V
DC Input Current	30mA
	-30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25L02XC Am25L03XC Am25L04XC T_A = 0°C to +75°C V_{CC} = 5.0V ±5%
 Am25L02XM Am25L03XM Am25L04XM T_A = -55°C to +125°C V_{CC} = 5.0V ±10%

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units	
V _{OH}	Output HIGH Voltage	V _{CC} = MIN., I _{OH} = -0.4mA V _{IN} = V _{IH} or V _{IL}	2.4	3.6		Volts	
V _{OL}	Output LOW Voltage (Note 2)	V _{CC} = MIN., I _{OL} = 4.92mA V _{IN} = V _{IH} or V _{IL}		0.15	0.3	Volts	
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts	
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts	
I _{IL}	Input LOW Current	V _{CC} = MAX., V _{IN} = 0.3V		-0.25	-0.4	mA	
I _{IH}	Input HIGH Current	V _{CC} = MAX., V _{IN} = 2.4V		2.0	20	μA	
	Input HIGH Current	V _{CC} = MAX., V _{IN} = 5.5V		4.0	40	μA	
I _{SC}	Output Short Circuit Current	V _{CC} = MAX., V _{OUT} = 0.0V	4.0	15	35	mA	
I _{CC}	Power Supply Current	V _{CC} = MAX.	Am25L02	XM	25	33	mA
				XC	25	35	
			Am25L03	XM	22	31	mA
				XC	22	33	
			Am25L04	XM	30	42	mA
				XC	30	45	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
 2. V_{OL}(MAX) = 0.3V with total device fanout of less than 90 Low Power TTL Unit Loads (36mA), otherwise, V_{OL}(MAX) = 0.35V.

Switching Characteristics (T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF)

Parameters	Description	Min.	Typ.	Max.	Units
t _{pd+}	Turn Off Delay CP to Output HIGH (except Q ₁₁ , Q ₁₁)	20	75	110	ns
t _{pd+}	Turn Off Delay CP to Q ₁₁ or Q ₁₁ HIGH	30	100	140	ns
t _{pd-}	Turn On Delay CP to Output LOW	20	75	100	ns
t _{s(D)}	Set-up Time Data Input	-15	8.0	20	ns
t _{s(S)}	Set-up Time Start Input	0	20	25	ns
t _{pd+(E)}	Turn Off Delay E to Q ₇ (11) HIGH		50	75	ns
t _{pd-(E)}	Turn On Delay E to Q ₇ (11) LOW		60	75	ns
t _{pwL} (CP)	Minimum LOW Clock Pulse Width		100	150	ns
t _{pwH} (CP)	Minimum HIGH Clock Pulse Width		70	100	ns
f _{max}	Maximum Clock Frequency	3.5	5.0		MHz

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Am25L02/L03/L04

Am25L02/3 TRUTH TABLE

Time	Inputs			Outputs																	
	\bar{D}	\bar{S}	\bar{E}	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	CC	
0	X	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D_7	H	L	X	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
2	D_6	H	L	D_7	D_7	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
3	D_5	H	L	D_6	D_7	D_6	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
4	D_4	H	L	D_5	D_7	D_6	D_5	L	H	H	H	H	H	H	H	H	H	H	H	H	H
5	D_3	H	L	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H	H	H	H	H	H	H	H	H
6	D_2	H	L	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H	H	H	H	H	H	H	H	H
7	D_1	H	L	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H	H	H	H	H	H	H	H	H
8	D_0	H	L	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H	H	H	H	H	H	H	H	H
9	X	H	L	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L	H	H	H	H	H	H	H	H
10	X	X	L	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L	H	H	H	H	H	H	H	H
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

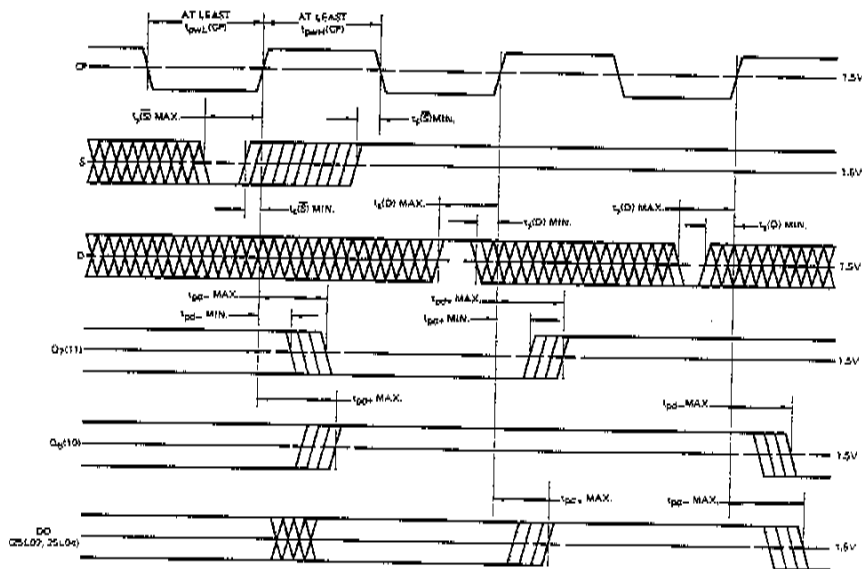
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 NC = No Change

Note: Truth Table for Am25L04 is extended to include 12 outputs.

USER NOTES FOR A/D CONVERSION

1. The register can be used with either current switches that require a low voltage level to turn the switch on, or current switches that require a high voltage level to turn the current switch on. If current switches are used which turn on with a low logic level the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If current switches are used that turn on with a high logic level then the digital output is active HIGH; a logic "1" is represented as a high voltage level.
2. For a maximum digital error of $\pm 1/2$ LSB the comparator must be biased. If current switches that require a low voltage level to turn on are used, the comparator should be biased $+1/2$ LSB and if the current switches require a high logic level to turn on then the comparator must be biased $-1/2$ LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion.
4. The register can be used to perform 2's complement conversion by offsetting the comparator $1/2$ full range $+1/2$ LSB and using the complement of the MSB Q_7 (11) as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the START input the OR function of CC and the appropriate register output.

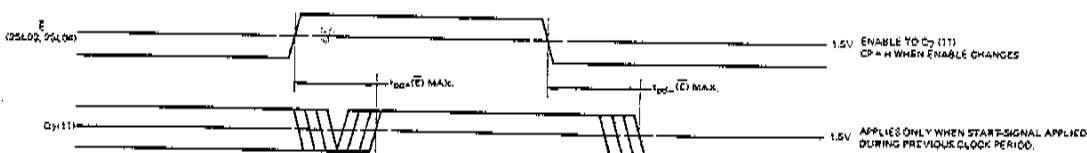
SWITCHING TIME WAVEFORMS



KEY TO TIMING DIAGRAM

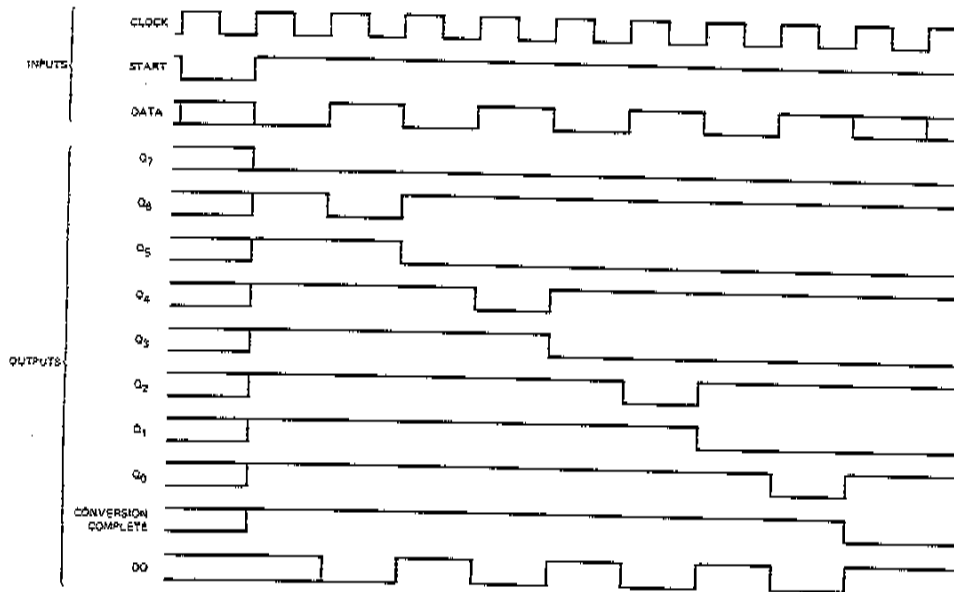
WAVEFORM	INPUTS	OUTPUTS
Horizontal line	MUST BE STEADY	WILL BE STEADY
Diagonal lines (top-left to bottom-right)	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
Diagonal lines (bottom-left to top-right)	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
Wavy lines	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

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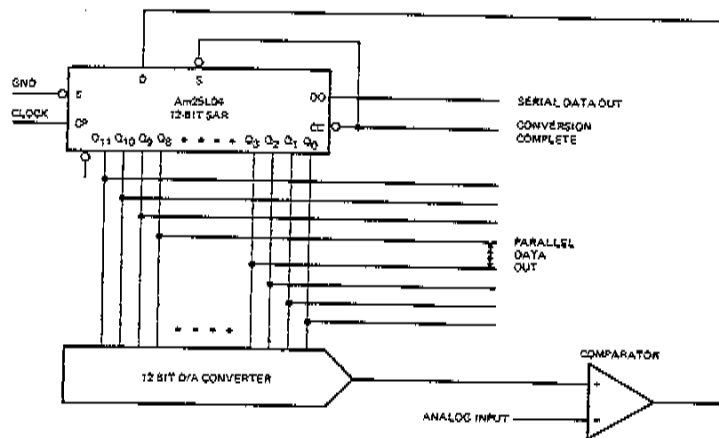
Am25L02/3 TIMING CHART



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3

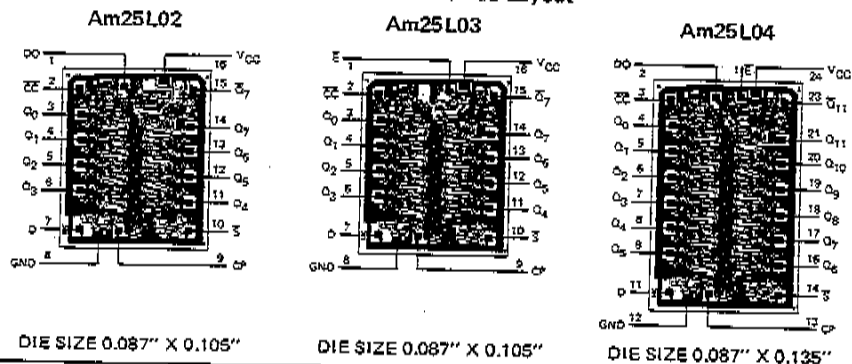
Am25L02/3/4 APPLICATION
Continuous Conversion Analog-to-Digital Converter



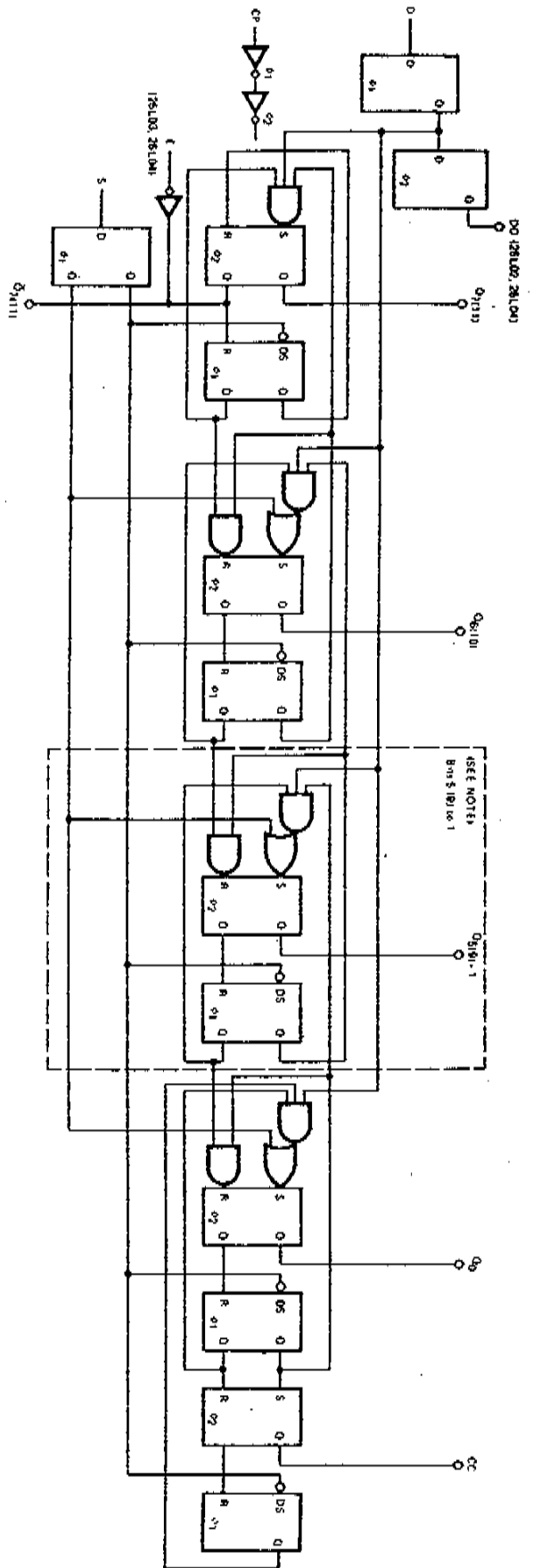
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This shows how the Am25L02/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a very high-speed continuous conversion Analog-to-Digital converter. Conversion time is limited mainly by the speed of the D/A converter and comparator with typical conversion rates of 300,000 conversions per second. The comparator can be the Am111 precision comparator, or Am106 high-speed comparator.

Metallization and Pad Layout

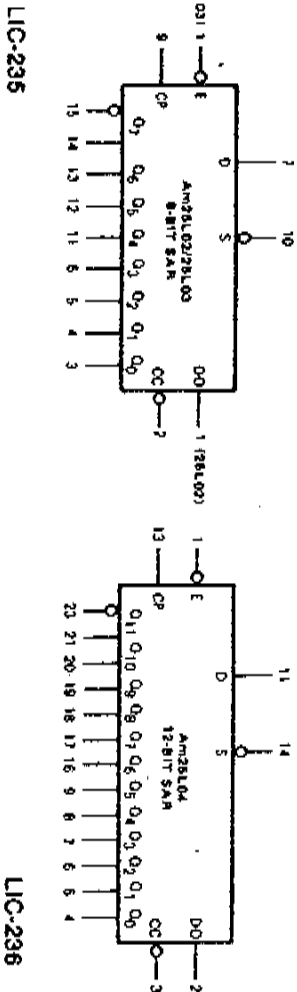


LOGIC DIAGRAMS



- Notes: 1. Cell logic is repeated for register stages. Q₅ to Q₁ Am25L02/3, Q₈ to Q₁ Am25L04.
- 2. Numbers in parentheses are for Am25L04.

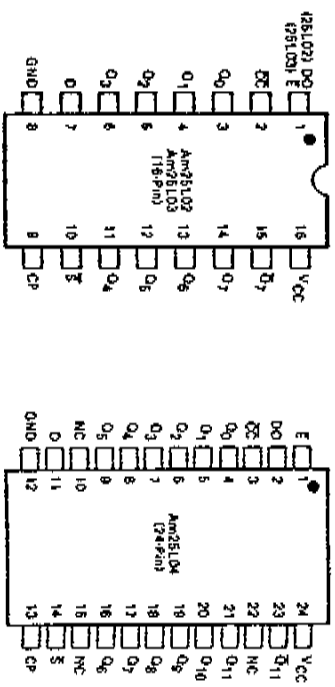
LOGIC SYMBOLS



VCC = Pin 16
GND = Pin 8

VCC = Pin 24
GND = Pin 12
NC = Pins 10, 15 22

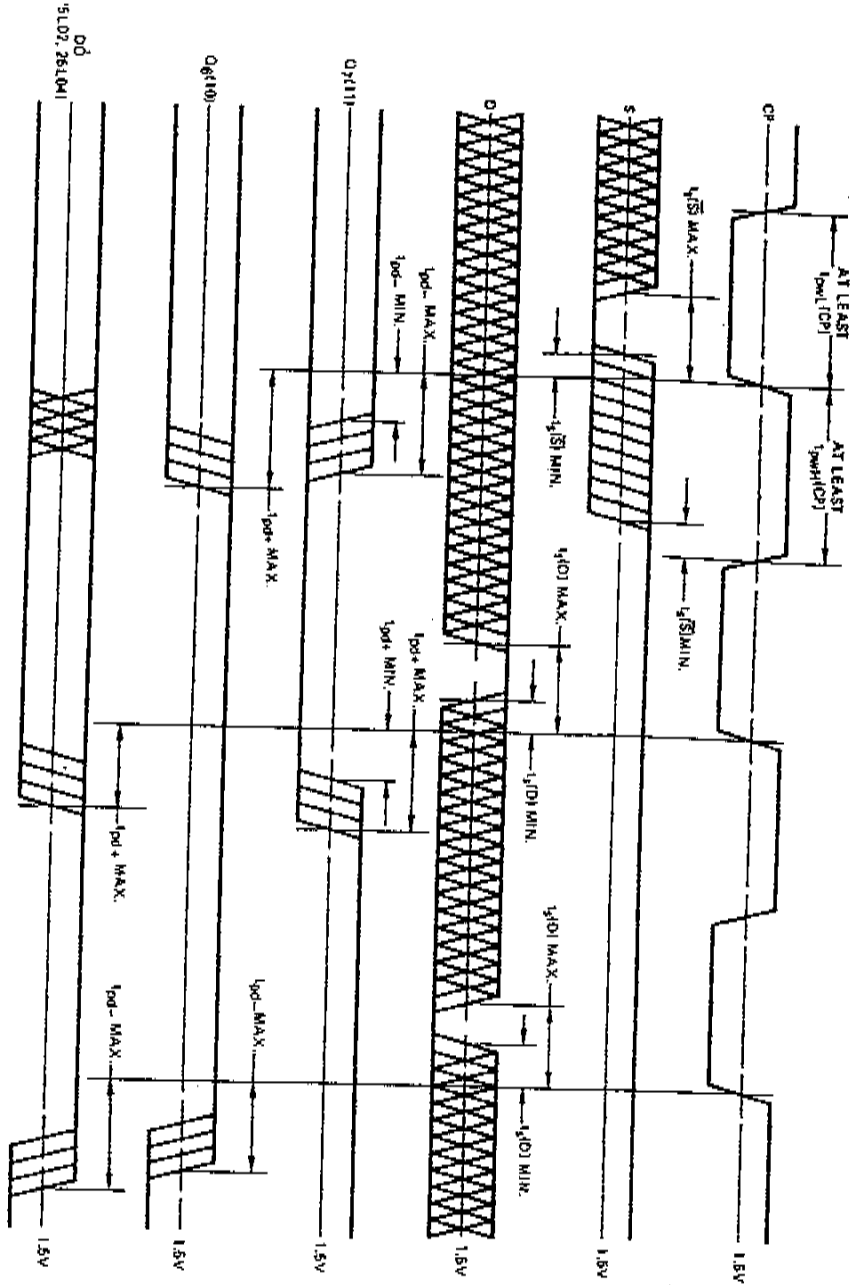
CONNECTION DIAGRAMS
Top Views



Note: Pin 1 is marked for orientation.

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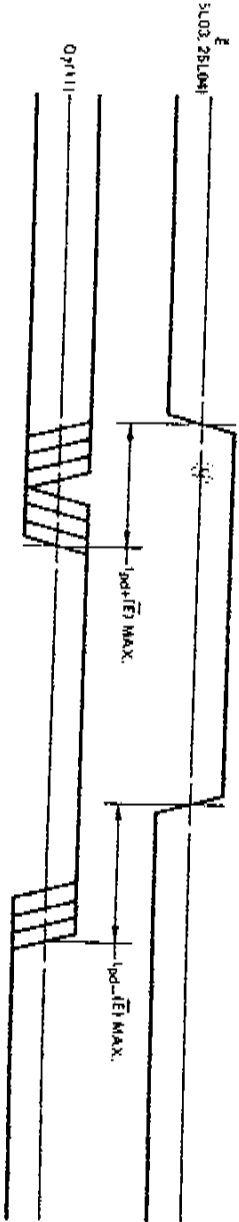
SWITCHING TIME WAVEFORMS



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN

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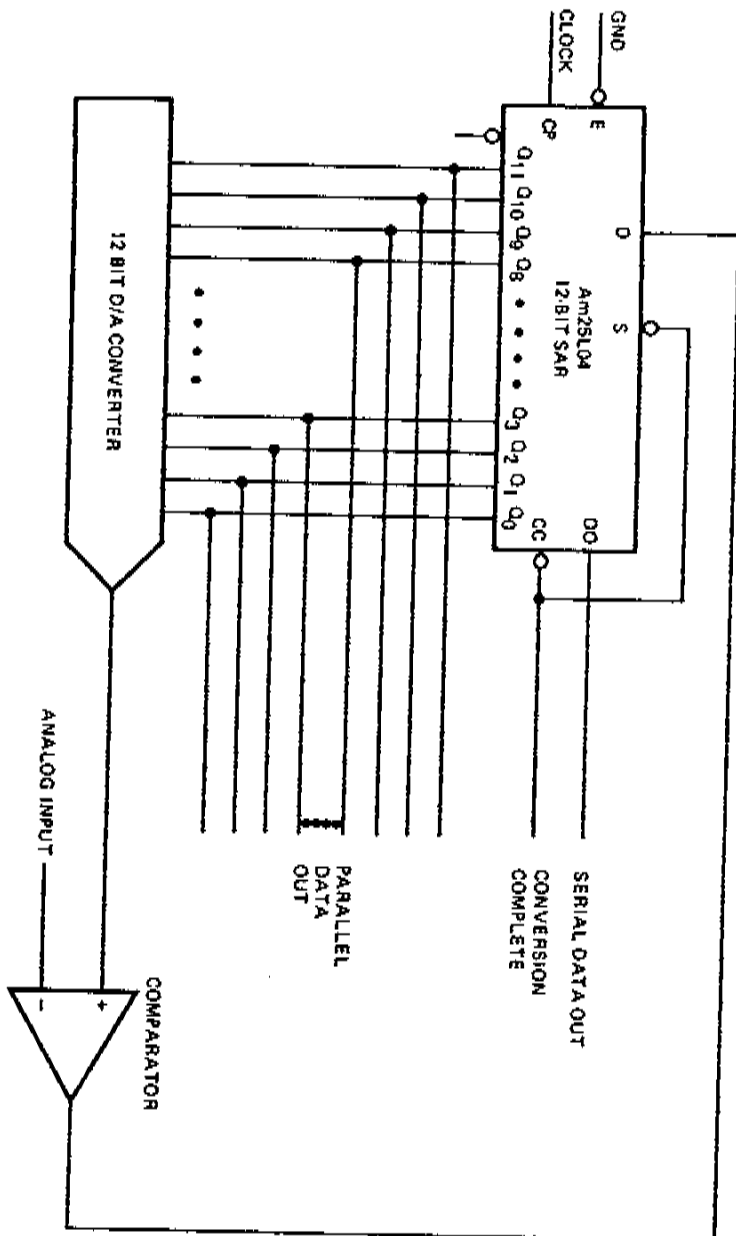


1.5V ENABLE TO O₇(111)
CP = H WHEN ENABLE CHANGES

1.5V APPLIES ONLY WHEN START-SIGNAL APPLIED DURING PREVIOUS CLOCK PERIOD.

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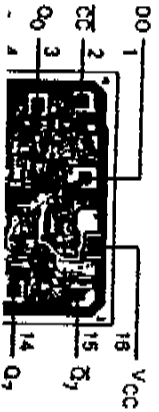
Am25L02/3/4 APPLICATION Continuous Conversion Analog-to-Digital Converter



This shows how the Am25L02/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a very continuous conversion Analog-to-Digital converter. Conversion time is limited mainly by the speed of the D/A converter and with typical conversion rates of 300,000 conversions per second. The comparator can be the Am111 precision comparator.

Metalization and Pad Layout

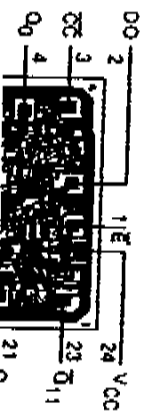
Am25L02

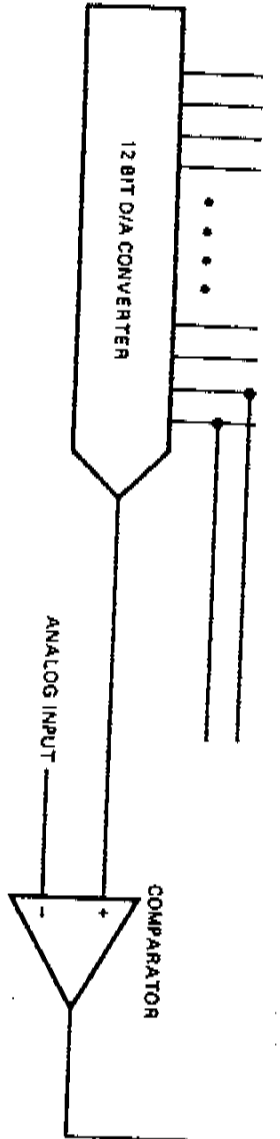


Am25L03



Am25L04



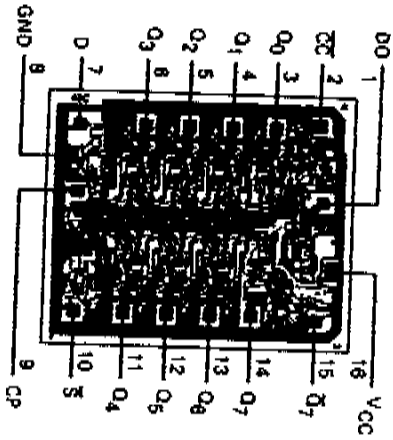


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how the Am25L02/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a very high-speed conversion Analog-to-Digital converter. Conversion time is limited mainly by the speed of the D/A converter and comparator conversion rates of 300,000 conversions per second. The comparator can be the Am111 precision comparator, or Am106 comparator.

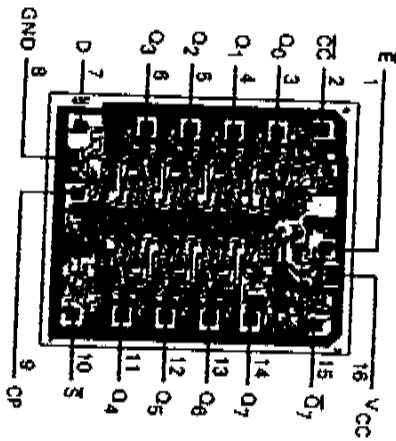
Metalization and Pad Layout

Am25L02



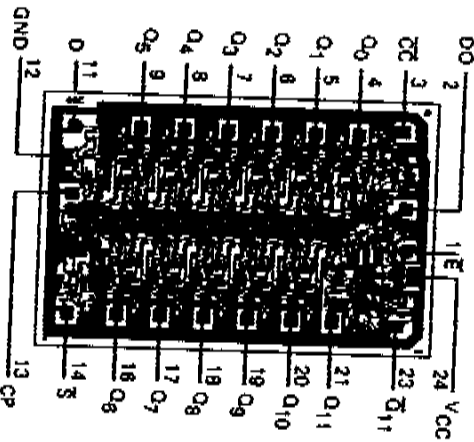
DIE SIZE 0.087" X 0.105"

Am25L03



DIE SIZE 0.087" X 0.105"

Am25L04



DIE SIZE 0.087" X 0.135"