TBA510

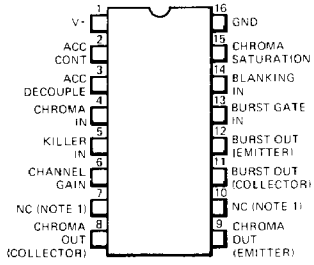
CHROMA PROCESSING CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA510 is a monolithic integrated circuit designed to perform the chrominance amplifier function for television receivers. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. A dc chroma gain control, which can be ganged to the receiver contrast control, is provided. Also incorporated is a variable gain automatic color control (ACC) stage, chroma blanking, burst gating, burst output stage. Two single output transistors provide burst and chroma output.

- **DC CHROMA CONTROL**
- **PAL DELAY LINE DRIVER**
- **ACC AMPLIFIER**
- **COLOR KILLER**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

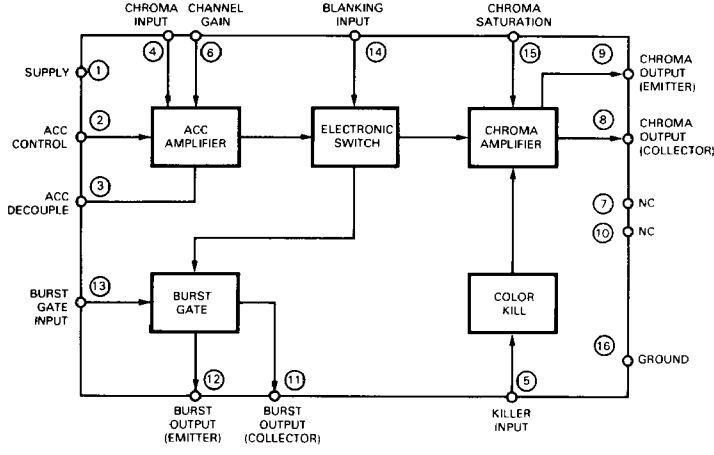
TYPE	PART NO.
510	TBA510
(510Q)	(TBA510Q)†

†Not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

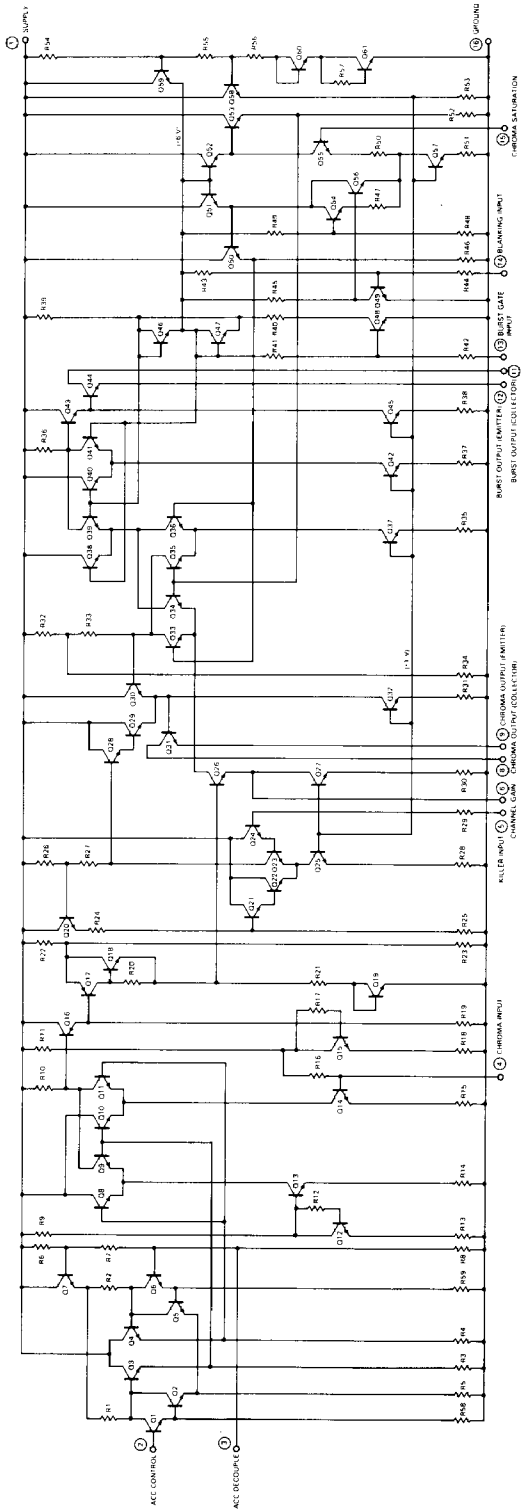
Supply Voltage	13.2 V
Internal Power Dissipation	550 mW
Current into Chroma Delay Line Driver (Collector)	20 mA
Current into Color Burst Output (Collector)	20 mA
Current out of Color Burst Output (Emitter)	20 mA
Current out of Chroma Delay Line Driver (Emitter)	20 mA
Operating Temperature Range	−20°C to +60°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT

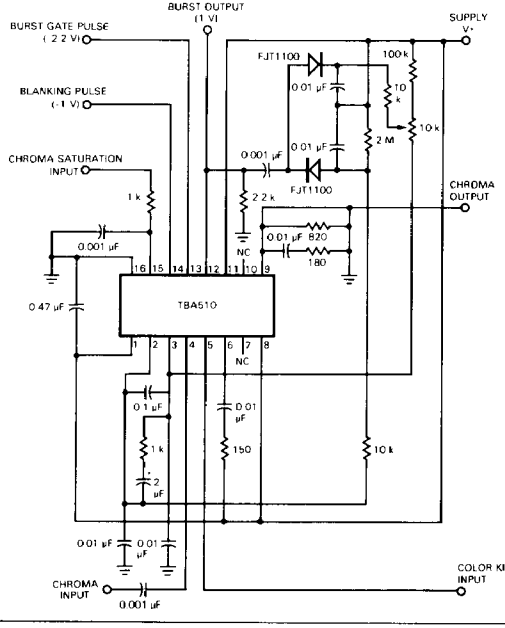


○ = Pin Numbers

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_+ = 12V$, See Test Circuit, unless otherwise specified.

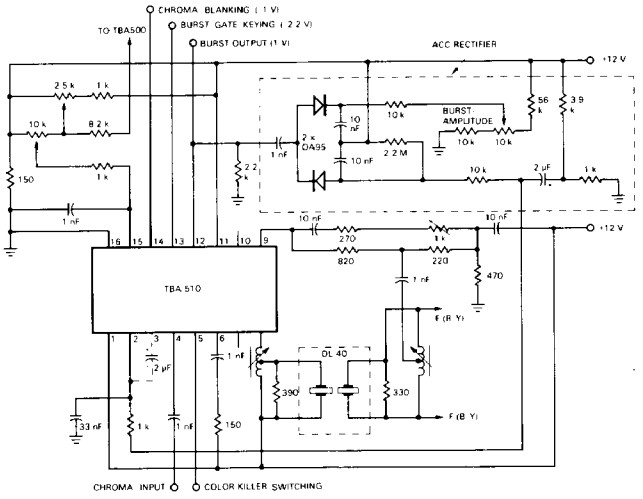
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Chroma Input (pin 4)					
Peak-to-Peak Signal at Chroma Input ($V_{4p\text{-}p}$)		15	150	300	$mV_{p\text{-}p}$
Input Impedance of Chroma Signal (Z_4)			3.0		kΩ
Burst Output (pin 11 and 12)					
DC Voltage at Color Burst Output (V_{12})			8.0		V
Peak-to-Peak Signal at Color Burst Output ($V_{12p\text{-}p}$)	(Note 2)		1.0		$V_{p\text{-}p}$
Collector Current of Color Burst Output (I_{11})			4.0		mA
Chroma Output (pin 8 and 9)					
DC Voltage at Chroma Output (V_9)			7.0		V
Peak-to-Peak Signal at Chroma Output ($V_{9p\text{-}p}$)	(Note 3)		1.0		$V_{p\text{-}p}$
Range of Contrast and Saturation Control		−30		+6.0	dB
Collector Current at Chroma Output (I_8)			5.0		mA
ACC Input (pin 2)					
ACC Input Voltage (V_2) for Maximum Gain (Note 4)			2.5		V
Input Impedance of ACC Control (Z_2)		50			kΩ
Chroma Saturation Control Input (pin 15)					
Control Voltage Range (V_{15}) (Note 4)		1.5		4.5	V
Input Impedance (Z_{15})		50			kΩ
Chroma Blanking Input (pin 14)					
Switching Level Range (V_{14})		−5.0		−1.0	V
Input Impedance (Z_{14})			2.0		kΩ
Burst Gate Input (pin 13)					
Switching Level Range (V_{13})		−5.0		−2.2	V
Input Impedance (Z_{13})			4.0		kΩ
Color Killer Input (pin 5)					
Input Voltage (V_5) for:					
Color on		2.5		4.0	V
Color off		0		1.8	V
Signal Suppression at Color Off		50			dB
Input Impedance (Z_5)		100			kΩ

TEST CIRCUIT



NOTES:
1. NC — no connection (not to be used as a tie point).
2. Color burst output kept constant by ACC circuit.
3. Chroma output (emitter) at nominal saturation and maximum contrast.
4. Gain control characteristic positive.

APPLICATION INFORMATION



The function is quoted against the corresponding pin number.

1. **Positive 12 V supply**
2. **A.C.C. control potential input**
   The potential required at pin 2 for maximum gain is about 2.5 V; gain reduction occurs when this potential is reduced; Zin > 50 kΩ.
3. **A.C.C. bias ripple compensation**
   The internal A.C.C. circuit consists of differential pair. The "cold" side is established internally at +2.5 V and is brought out on pin 3. This enables a decoupling capacitor to be connected and returned to the point which secures the lowest supply line ripple amplitude injection into the A.C.C. loop.
4. **Chroma signal input**
   The allowable input voltage range is from 15 mV to 300 mV peak-to-peak with a color bar signal. The input impedance is greater than 2 kΩ.
5. **Color killer switching input**
   The input impedance is greater than 50 kΩ. Color "on" 2.5 to 4 V; color "off" 0 to 1.8 V. The chroma signal suppression when killed is greater than 50 dB.
6. **Emitter decoupling network**
   The series network decouples an emitter of an amplifier stage in the chroma channel. The value of resistance influences the chroma channel gain.
7. **No connection**
   Not to be used as a tie point. It is recommended that pins 7 and 10 be grounded.
8. **Delay line driver (collector)**
   Supplies the chroma signal drive to the delay line driver transformer, the "cold" end of which is connected to +12 V. The maximum permitted voltage excursion at this pin is 20 V peak. Maximum current, 12 mA peak.
9. **Delay line driver (emitter)**
   Supplies the chroma to the network which provides the non-delayed signal to the delay line output transformer. The emitter is established internally at a potential of 6.8 ± 1.0 V and the external network, which must incorporate a resistive dc path to ground, must not demand more than 20 mA peak current.
10. **No connection**
    Not to be used as a tie point. (See pin 7.)
11. **Color burst output (collector)**
    If a low impedance color burst is required (from the emitter of the color burst output, pin 12) pin 11 will be connected to the +12 V supply. The maximum voltage and current excursions permitted on pin 11 are 20 V peak and 20 mA peak.
12. **Color burst output (emitter)**
    An external load resistor of 2.0 kΩ is required connected to ground and dc potential of 7.7 ± 1.0 V is established on pin 12 due to the internal circuitry. The burst output voltage is 1.0 V peak-to-peak.
13. **Burst gate gating pulse**
    The horizontal flyback pulse can be used as a source of gating waveform. A negative-going pulse of not greater than 5.0 V amplitude is necessary, the input impedance is 4.0 kΩ and the switching level is between −2.2 V and −5.0 V.
14. **Chroma blanking pulse input**
    A negative going horizontal flyback pulse can be used here. Its amplitude should not exceed −5.0 V. The input impedance at this pin is 2.0 kΩ and the switching level is about −1.0 V. During scan time, the dc voltage on this pin should not be negative.
15. **Chroma saturation control**
    The dc control voltage range required is from 1.5 to 4.5 V (highest gain at 4.5 V). The input impedance is > 50 kΩ and a control range from +6.0 to −30 dB is given.
16. **Ground**