LED DISPLAY/INTERFACE CIRCUIT

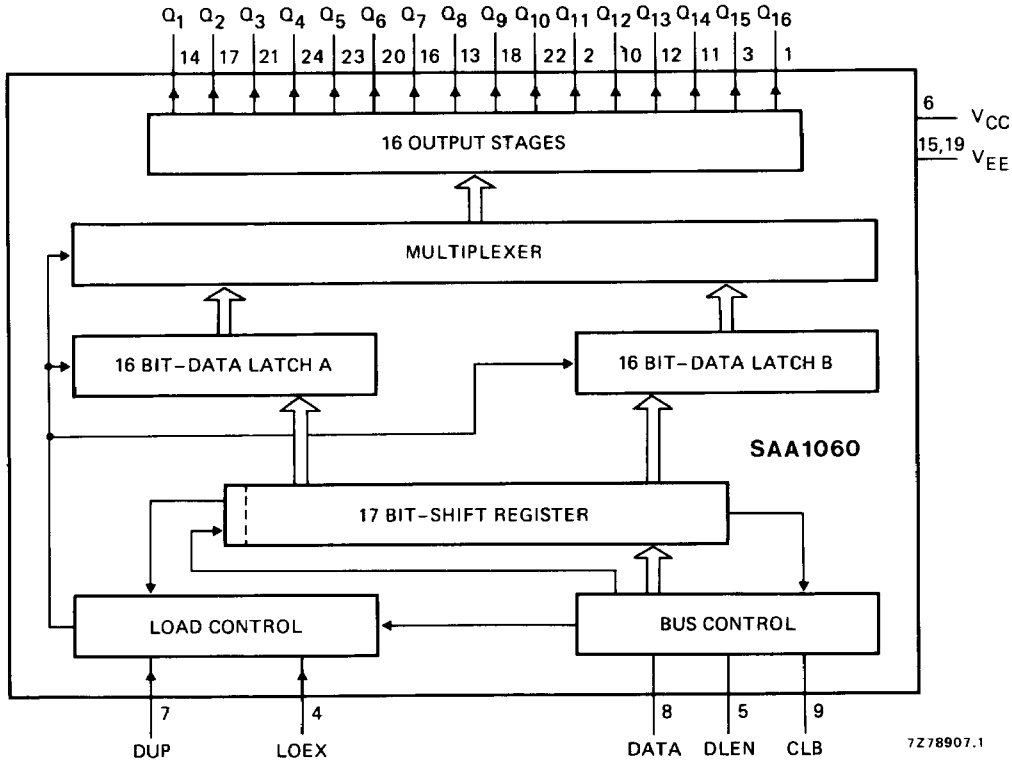

Fig. 1 Block diagram.

Features

- Driving 7, 14, 16-segment displays.
- Driving linear displays, bar graph displays for analogue functions.
- Serial to parallel decoder.
- Bus control for the selection of 18-bit words.
- 2 x 16-bit latch.
- Duplex operation for two modes of output: static (16 bit) or dynamic (2 x 16 bit).
- Data transfer control.
- 2 outputs for higher output current (80 mA).

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		4 to 6 V
Operating ambient temperature range	T_{amb}		−20 to + 80 °C
Maximum input frequency	f_I	typ.	50 kHz
Supply current	I_{CC}	typ.	60 mA
Output current	I_O	<	40 mA
Output current (Q_8 and Q_{16} only)	I_O	<	80 mA

PACKAGE OUTLINE

24-lead DIL; plastic (SOT101A).

GENERAL DESCRIPTION

The integrated circuit SAA1060 is primarily designed to drive the display unit of a digital tuning system. It can also be used as a 16-bit serial to parallel decoder. Since the device has no decoder (this is handled by a microcomputer), it has many applications:

- driving 7-segment displays
- driving 14-segment displays
- driving linear displays, e.g. pointer, bar graph
- static output of switch-functions
- digital to analogue converter, with external R-2R network
- extension of the number of outputs for microprocessors or microcomputers.

Data transmission is initiated by means of a burst of clock pulses (CLB), a data line enable signal (DLEN) and the data signal (DATA). The bus control circuit distinguishes between interference and valid data by checking word length (17 bits) and the leading zero. This allows different bus information to be supplied on the same bus lines for other circuits (e.g. SAA1056 with 16 bits).

The last bit (bit 17) of the data word contains the information which of the two internal latches will be loaded. The input LOEX determines if the latched data of selected latches is presented directly to the outputs, or synchronized with the data select signal DUP.

The output stages are n-p-n transistors with open collectors. The current capability is designed for the requirements of duplex operation. Two of the outputs (Q_8 and Q_{16}) are arranged for double current, so that 2 x 2 segments can be connected in parallel.

OPERATION DESCRIPTION

Data inputs (DLEN, DATA)

The SAA1060 processes serially the 18-bit data words synchronized with the clock burst (CLB) and applied to the data input DATA. A command will be accepted only when the data line enable input (DLEN) is HIGH (see Fig. 3).

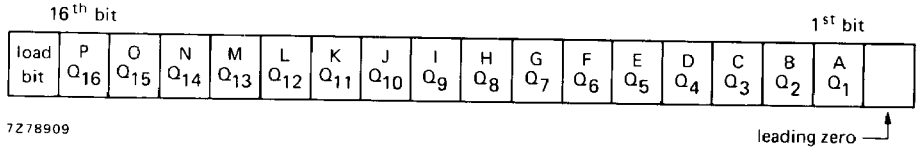

Fig. 2 Organization of a data word.

Condition for 17th bit:
0 = load data latch B
1 = load data latch A

The loading of the accepted information in one of the data latches is done by the 19th clock pulse, when DLEN is LOW.

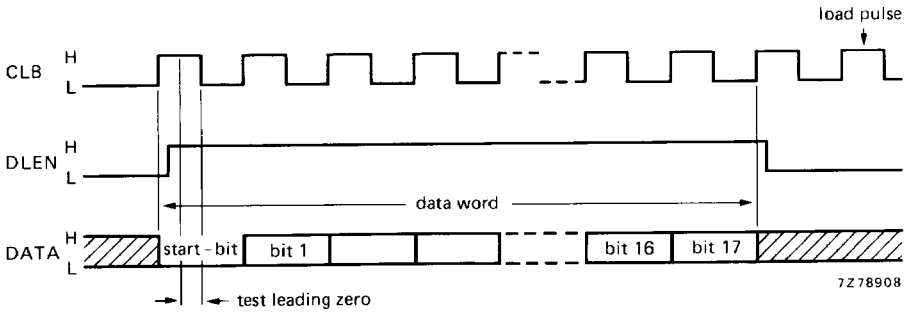

Fig. 3 Pulse diagram of the 16-bit data transmission.

Each data word must start with a leading zero. The SAA1060 checks the data word for the correct length (18 bits) and also for the leading zero.
The actual data is switched directly to the appropriate outputs. For switching on a segment, a '0' (LOW) is necessary at the appropriate data bit.

Data selection input (DUP)

The logic states at input DUP determine which of the two latch contents can be found on the output.

0 = latch A contents
1 = latch B contents

Load control input (LOEX)

Input LOEX determines the operation mode in which the device is able to work.

0 = duplex mode, i.e. output synchronized with the duplex signal
1 = d.c. mode, i.e. output direct from the by DUP selected data latch.

When operating in duplex mode at 50 Hz, the time between two data words to be transmitted must be > 21 ms.

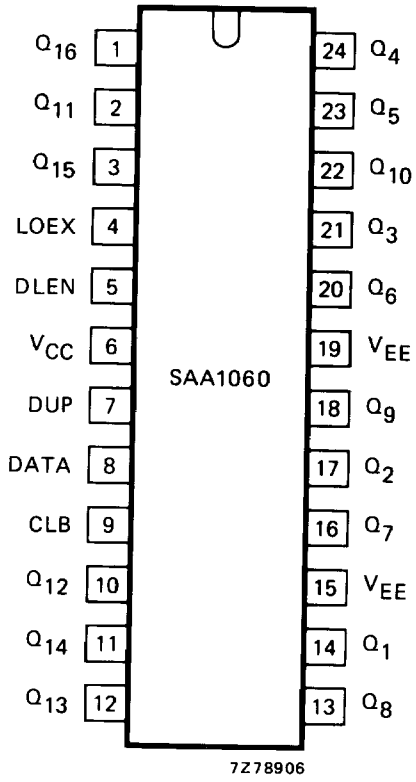

Fig. 4 Pinning diagram.

RATINGS (V_{EE} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{CC}	−0,3 to + 7	V
Total power dissipation	P_{tot}	max. 900	mW
Operating ambient temperature range	T_{amb}	−20 to + 80	°C
Storage temperature range	T_{stg}	−25 to + 125	°C

CHARACTERISTICS

V_{EE} = 0; T_{amb} = 25 °C; unless otherwise specified

	V_{CC} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{CC}	4	5	6	V	
Supply current	5	I_{CC}	–	60	–	mA	
Inputs DATA, CLB, DLEN, LOEX							
input voltage HIGH	5	V_{IH}	2	–	5	V	
input voltage LOW	5	V_{IL}	–	–	1	V	
input current LOW	5	$-I_{IL}$	–	–	20	μA	V_I = 0
maximum input frequency	5	f_I	–	50	–	kHz	
Input DUP							
input voltage HIGH	5	V_{IH}	0,8	–	12	V	
input voltage LOW	5	V_{IL}	–6	–	0,4	V	
input current HIGH	5	I_{IH}	0,01	–	12	mA	
maximum input frequency	5	f_I	–	50	–	kHz	
Outputs Q_1 to Q_7, Q_9 to Q_{15}							
output voltage HIGH	5	V_{QH}	–	–	16,8	V	I_{QH} = 0
output voltage LOW	5	V_{QL}	–	–	0,5	V	I_{QL} = 40 mA
output current LOW							
duplex mode	5	I_{QL}	–	–	60	mA	peak value at sinusoidal voltage
d.c. mode	5	I_{QL}	–	20	40	mA	
Outputs Q_8 and Q_{16}							
output voltage HIGH	5	V_{QH}	–	–	16,8	V	I_{QH} = 0
output voltage LOW	5	V_{QL}	–	–	0,5	V	I_{QL} = 80 mA
output current LOW							
duplex mode	5	I_{QL}	–	–	120	mA	peak value at sinusoidal voltage
d.c. mode	5	I_{QL}	–	40	80	mA	