- **Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages**
- **Dependable Texas Instruments Quality and Reliability**

description

These monolithic, edge-triggered J-K flip-flops feature gated inputs, direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse, and after the clock input threshold voltage has been passed, the gated inputs are locked out.

These flip-flops are ideally suited for medium-to-high-speed applications and can result in a significant saving in system power dissipation and package count where input gating is required.

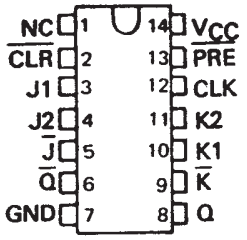
The SN5470 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN7470 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

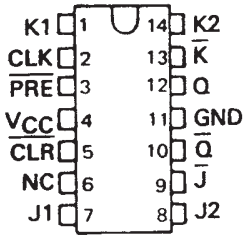
INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	L	X	X	H	L
H	L	L	X	X	L	H
L	L	X	X	X	L†	L†
H	H	↑	L	L	Q_0	Q_0
H	H	↑	H	L	H	L
H	H	↑	L	H	L	H
H	H	↑	H	H	TOGGLE	
H	H	L	X	X	Q_0	Q_0

If inputs J and K are not used, they must be grounded. Preset or clear function can occur only when the clock input is low.
†This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

SN5470 . . . J PACKAGE
SN7470 . . . N PACKAGE
(TOP VIEW)

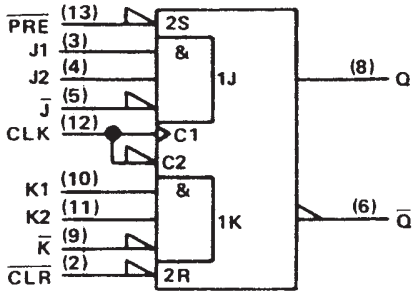


SN5470 . . . W PACKAGE
(TOP VIEW)



NC - No internal connection

logic symbol†

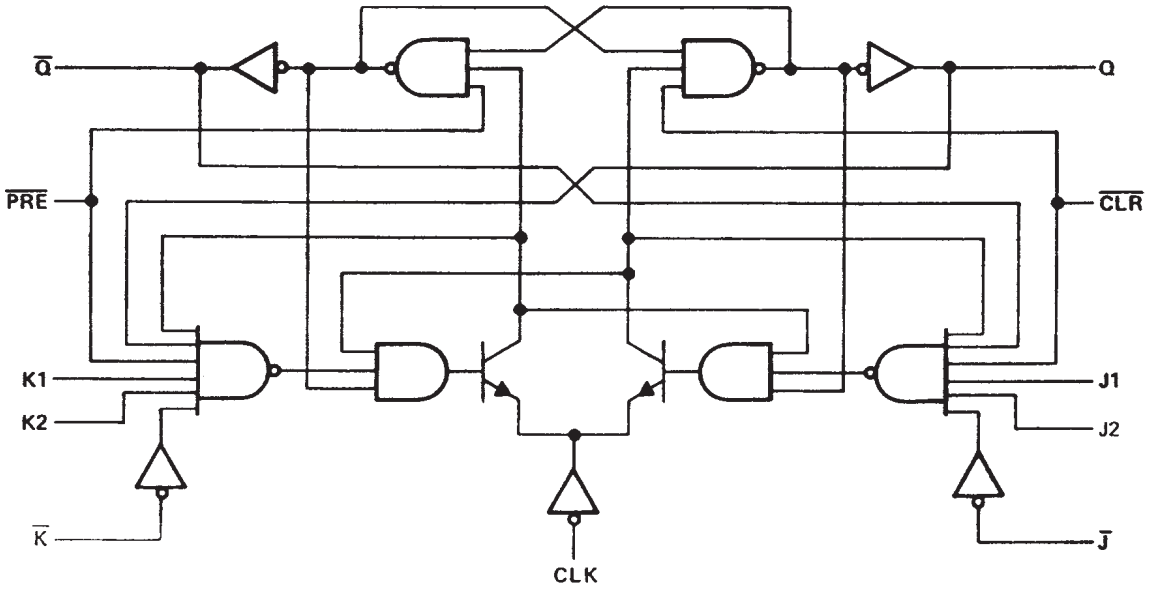


†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages only.

positive logic

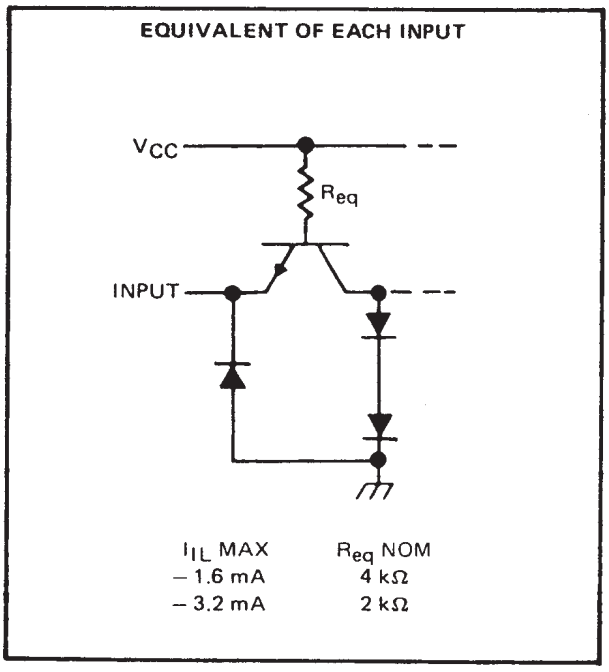
$$J = J1 \cdot J2 \cdot \overline{J}$$
$$K = K1 \cdot K2 \cdot \overline{K}$$

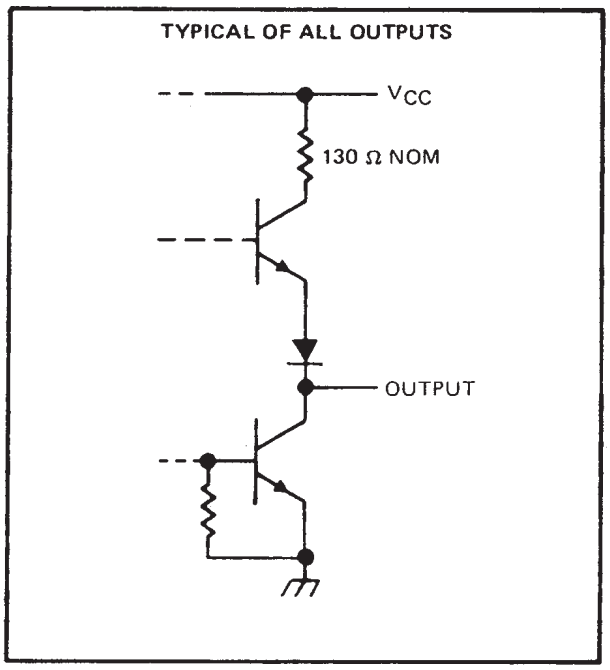
logic diagram (positive logic)



'70-GATED J-K WITH CLEAR AND PRESET

schematics of input and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature: SN5470 . . . . . −55°C to 125°C
SN7470 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

			SN5470			SN7470			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				16			16	mA
t_w	Pulse duration	CLK high	20			20			ns
		CLK low	30			30			
		$\overline{PRE}$ or $\overline{CLR}$ low	25			25			
t_{su}	Setup time before CLK↑		20			20			ns
t_h	Hold time-Data after CLK↑		5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN5470			SN7470			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	$\overline{PRE}$ or $\overline{CLR}$	V_{CC} = MAX,	V_I = 2.4 V			80			80	μA
	All other					40			40	
I_{IL}	$\overline{PRE}$ or $\overline{CLR}$¶	V_{CC} = MAX,	V_I = 0.4 V			−3.2			−3.2	mA
	All other					−1.6			−1.6	
I_{OS}§		V_{CC} = MAX		−20		−57	−18		−57	mA
I_{CC}		V_{CC} = MAX,	See Note 2		13	26		13	26	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
¶Clear is tested with preset high and preset is tested with clear high.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 400 Ω, C_L = 15 pF	20	35		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$				50	ns
t_{PHL}						50	ns
t_{PLH}	CLK	Q or $\overline{Q}$			27	50	ns
t_{PHL}					18	50	ns

†f_{max} = maximum clock frequency; t_{PLH} = propagation delay time, low-to-high level output; t_{PHL} = propagation delay time, high-to-low level output.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN5470J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SN7470N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN7470N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SNJ5470J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SNJ5470J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SNJ5470W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	-55 to 125		
SNJ5470W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF SN5470, SN7470 :

- Catalog: SN7470
- Military: SN5470

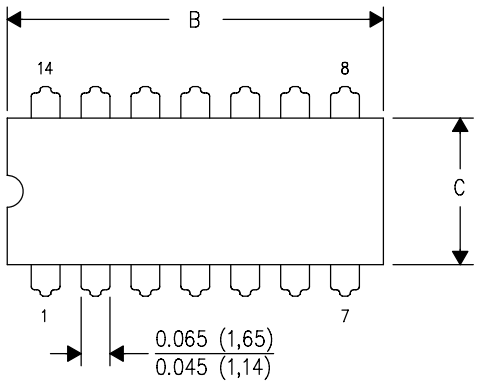
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

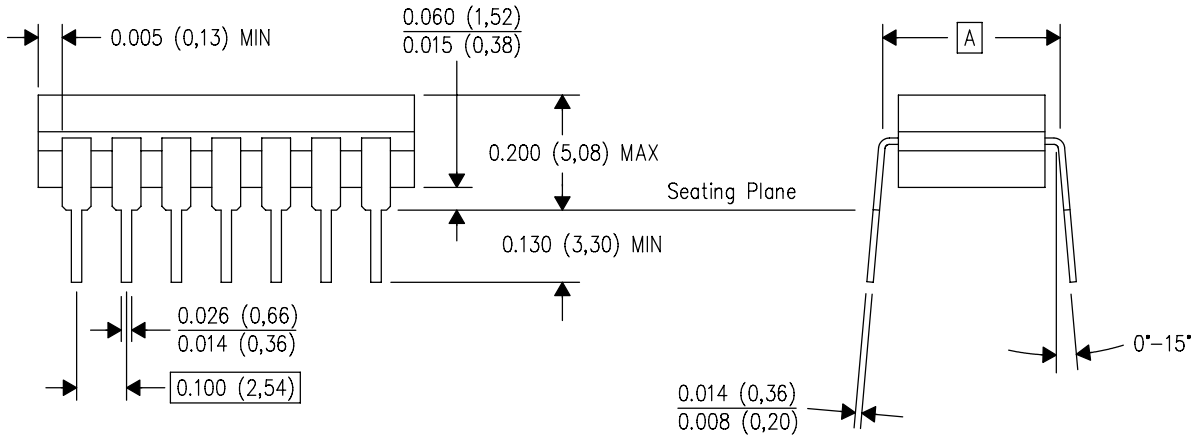
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



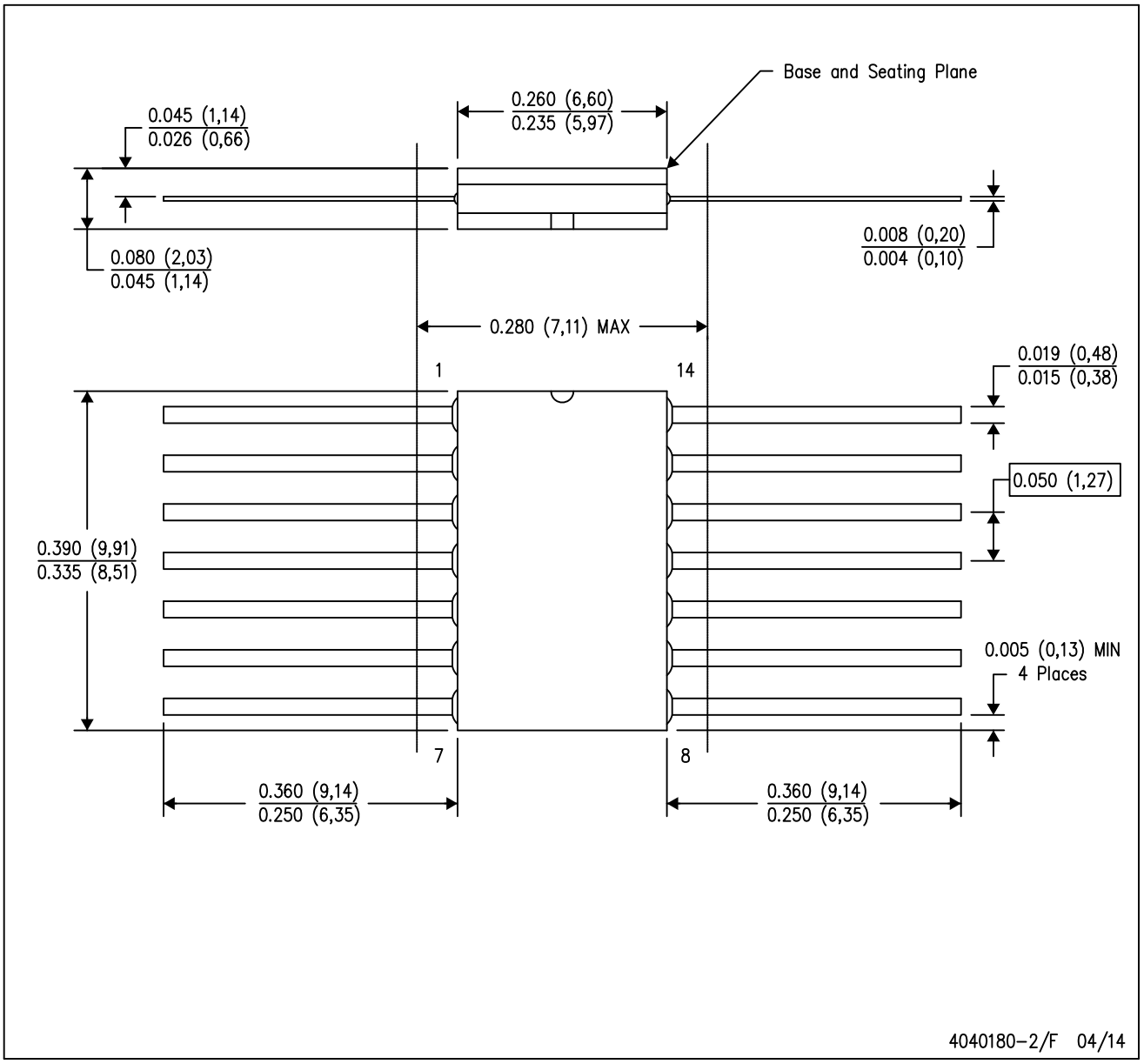
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

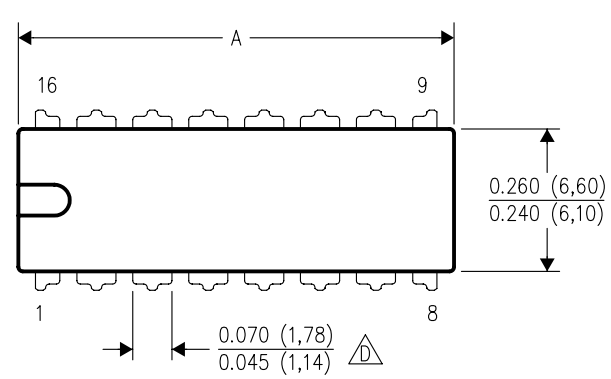


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

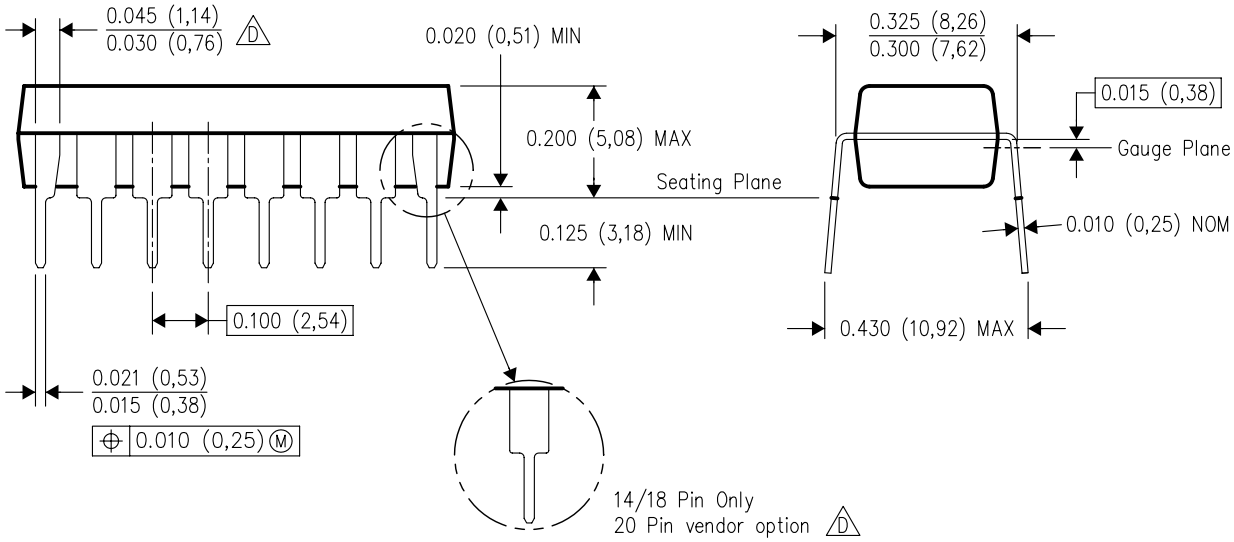
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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