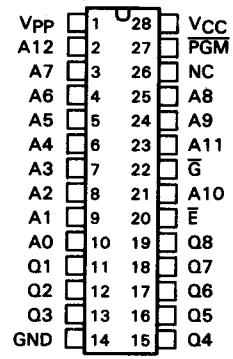
JULY 1983 – REVISED MARCH 1988

- **Organization . . . 8192K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible with Existing 64K EPROMs**
- **All Inputs and Outputs are TTL Compatible**
- **Max Access/Min Cycle Time**

TMS2764-17	**170 ns**
TMS2764-20	**200 ns**
TMS2764-25	**250 ns**
TMS2764-45	**450 ns**

- **Low Standby Power Dissipation . . . 184 mW (Maximum)**
- **JEDEC Approved Pinout**
- **21-V Power Supply Required for Programming**
- **Fast Programming Algorithm**
- **N-Channel Silicon-Gate Technology**
- **PEP4 Version Available with 168 Hour Burn-In and Guaranteed Operating Temperature Range from −10°C to 85°C (TMS2764-_ _JP4)**

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A12	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	21-V Power Supply

description

The TMS2764 is an ultraviolet-light erasable, electrically programmable read-only memory. It has 65,536 bits organized as 8,192 words of 8-bit length. The TMS2764 only requires a single 5-volt power supply with a tolerance of ±5%.

The TMS2764 provides two output control lines: Output Enable ($\overline{G}$) and Chip Enable ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in microprocessor systems. The TMS2764 has a power-down mode that reduces maximum power dissipation from 150 mA to 35 mA when the device is placed on standby.

This EPROM is supplied in a 28-pin, 15,2-mm (600-mil) dual-in-line ceramic package and is designed for operation from 0°C to 70°C. The TMS2764 is also offered in the PEP4 version with an extended guaranteed operating temperature range of −10°C to 85°C and 168 hour burn-in (TMS2764-_ _JP4).

operation

The six modes of operation for the TMS2764 are listed in the following table.

FUNCTION (PINS)	MODE					
	Read	Output Disable	Power Down (Standby)	Fast Programming	Program Verification	Inhibit Programming
$\overline{E}$ (20)	V_{IL}	X†	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}$ (22)	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X†
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X†	V_{IL}	V_{IH}	X†
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP} or V_{CC}
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
Q1-Q8 (11 to 13, 15 to 19)	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z

†X = V_{IH} or V_{IL}

read/output disable

The two control pins ($\overline{E}$ and $\overline{G}$) must have low-level TTL signals in order to provide data at the outputs. Chip enable ($\overline{E}$) should be used for device selection. Output enable ($\overline{G}$) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum active current from 150 mA to 35 mA. A TTL high-level signal applied to $\overline{E}$ selects the power-down mode. In this mode, the outputs assume a high-impedance state, independent of $\overline{G}$.

erasure

Before programming, the TMS2764 is erased by exposing the chip to shortwave ultraviolet light that has a wavelength of 253.7 nanometers (2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 mW/cm^2 UV lamp will erase the device in approximately 20 minutes. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are at a high level. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS2764, the window should be covered with an opaque label.

Fast programming

Note that the application of a voltage in excess of 22 V to V_{PP} may damage the TMS2764.

After erasure, logic 0s are programmed into the desired locations. Programming consists of the following sequence of events. With the level on V_{PP} equal to 21 V and $\overline{E}$ at TTL low, data to be programmed is applied in parallel to output pins Q1-Q8. The location to be programmed is addressed. Once data and addresses are stable, a TTL low-level pulse is applied to $\overline{PGM}$. Programming pulses must be applied at each location that is to be programmed. Locations may be programmed in any order.

Programming uses two types of programming pulse: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each application, the byte being programmed is verified. If the correct data is read, the Final programming pulse is then applied. If correct data is not read, a further 1 millisecond programming pulse is applied up to a maximum X of 15. The Final programming pulse is 4X milliseconds long. This sequence of programming pulses and byte verification is done at V_{CC} = 6.0 V and V_{PP} = 21.0 V. When the full Fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V. A flowchart of the Fast programming routine is shown in Figure 1.

multiple device programming

Several TMS2764s can be programmed simultaneously by connecting them in parallel and following the programming sequence previously described.

program inhibit

The program inhibit is useful when programming multiple TMS2764s connected in parallel with different data. Program inhibit can be implemented by applying a high-level signal to $\overline{E}$ or $\overline{PGM}$ of the device that is not to be programmed.

program verify

Programmed bits may be verified with V_{PP} = 21 V when $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL} and $\overline{PGM}$ = V_{IH}.

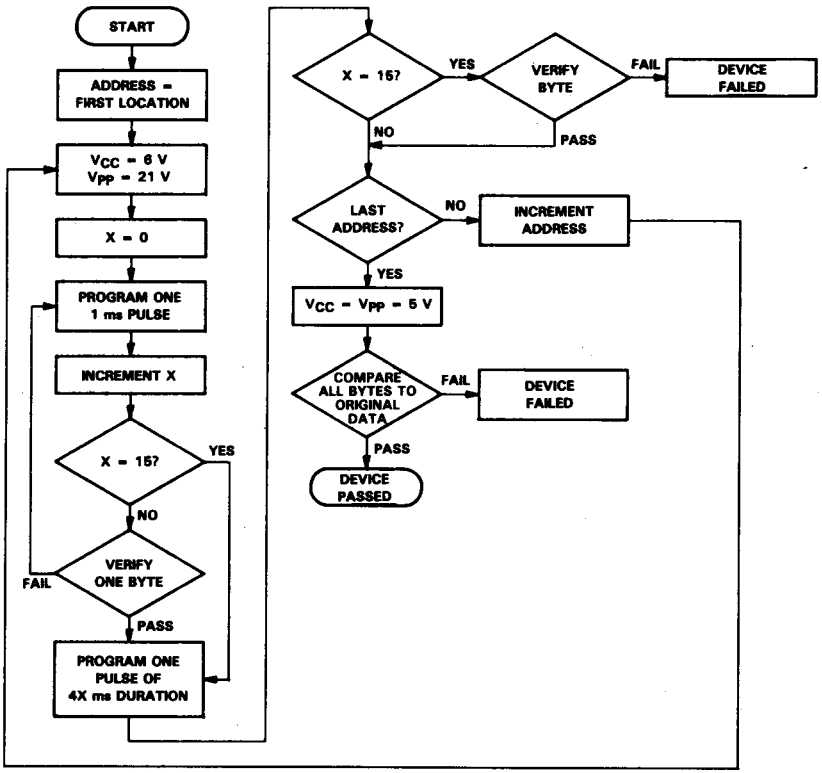
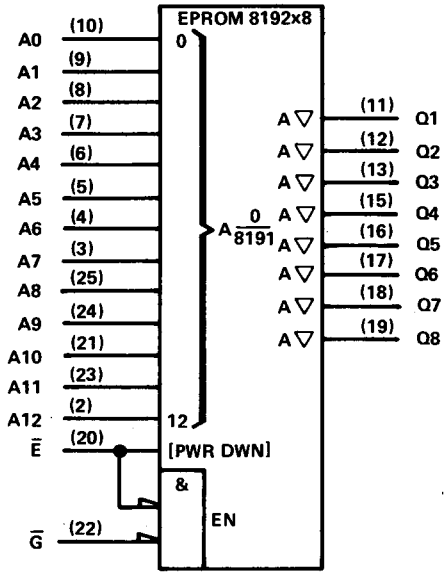


FIGURE 1. FAST PROGRAMMING FLOWCHART

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} . . . . . −0.6 V to 22 V
Input voltage range . . . . . −0.6 V to 7 V
Output voltage range . . . . . −0.6 V to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{PP}	Supply voltage		V_{CC}		V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 1)	−0.1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 1: The algebraic convention, where the more negative (less positive) limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA		0.45	V
I_I	Input current (load)	V_I = 0 V to 5.25 V		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.25 V		±10	μA
I_{PP1}	V_{PP} supply current (read)	V_{PP} 5.25 V		15	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{E}$ and $\overline{PGM}$ at V_{IL}		50	mA
I_{CC1}	V_{CC} supply current (standby)	$\overline{E}$ at V_{IH}		35	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{E}$ and $\overline{G}$ at V_{IL}		150	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER		TEST CONDITIONS	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V	6	9	pF
C_o	Output capacitance	V_O = 0 V	8	12	pF

†Capacitance measurements are made on a sample basis only.
‡Typical values are at T_A = 25°C and nominal voltage.

switching characteristics over recommended supply voltage range and operating free-air temperature range, C_L = 100 pF, 1 Series 74 TTL load (see Note 2 and Figure 2)

PARAMETER		TMS2764-17		TMS2764-20		TMS2764-25		TMS2764-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		170		200		250		450	ns
$t_{a(E)}$	Access time from $\overline{E}$		170		200		250		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		65		75		100		150	ns
$t_{dis(G)}$§	Output disable time from $\overline{G}$	0	60	0	60	0	85	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first	0		0		0		0		ns

NOTE 2: For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output timing reference levels are 0.8 V and 2.0 V.
§Value calculated from 0.5 V delta to measured output level; $t_{dis(G)}$ is specified from $\overline{G}$ or $\overline{E}$, whichever occurs first. Refer to read-cycle timing diagram. This parameter is only sampled and not 100% tested.

recommended conditions for Fast programming routine, T_A = 25°C (see Note 2 and Fast programming cycle time diagram)

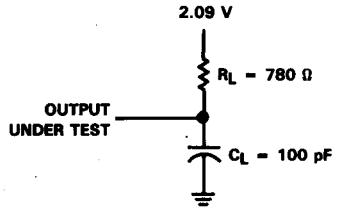
PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)	5.75	6	6.25	V
V_{PP}	Supply voltage (see Note 4)	20.5	21	21.5	V
$t_{w(IPGM)}$	$\overline{PGM}$ initial program pulse duration (see Note 5)	0.95	1	1.05	ms
$t_{w(FPGM)}$	$\overline{PGM}$ final pulse duration (see Note 6)	3.8		63	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{su(E)}$	$\overline{E}$ setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs

Fast programming characteristics, T_A = 25°C (see Note 2 and Fast programming cycle timing diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{dis(G)FP}$	Output disable time from $\overline{G}$ (see Note 7)	C_L = 100 pF	0		130	ns
$t_{en(G)FP}$	Output enable time from $\overline{G}$	1 Series 74 TTL Load			150	

NOTES: 2. For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output timing reference levels are 0.8 V and 2.0 V.
3. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
4. When programming the TMS2764, connect a 0.1 μF capacitor between V_{PP} and GND to suppress spurious voltage transients which may damage the device.
5. The Initial program pulse duration tolerance is 1 ms ±5%.
6. The length of the Final pulse will vary from 3.8 ms to 63 ms depending on the number of Initial pulse applications (X).
7. This parameter is only sampled and is not 100% tested.

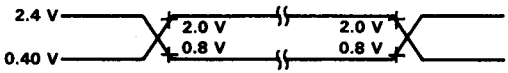
PARAMETER MEASUREMENT INFORMATION



NOTE 8: $t_f \leq 20$ ns and $t_r \leq 20$ ns.

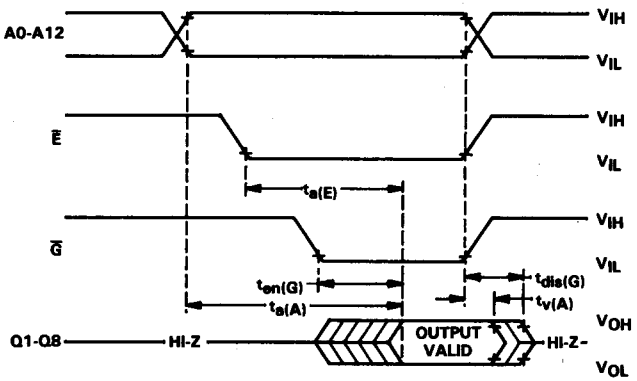
FIGURE 2. TYPICAL OUTPUT LOAD CIRCUIT

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 for logic 1 and 0.4 V for logic 0. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 for both inputs and outputs.

read cycle timing



fast program cycle timing