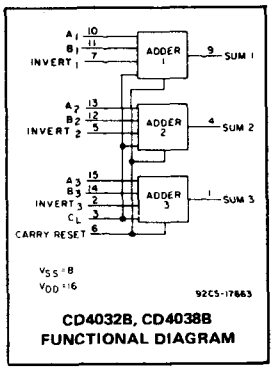
CMOS Triple Serial Adders

High-Voltage Types (20-Volt Rating)
Positive Logic Adder — CD4032B
Negative Logic Adder — CD4038B

The RCA-CD4032B and CD4038B types consist of three serial adder circuits with common CLOCK and CARRY-RESET inputs. Each adder has provisions for two serial DATA INPUT signals and an INVERT command signal. When the command signal is a logical "1", the sum is complemented. Data words enter the adder with the least significant bit first; the sign bit trails. The output is the MOD 2 sum of the input bits plus the carry from the previous bit position. The carry is only added at the positive-going clock transition for the CD4032B or at the negative-going clock for the CD4038B, thus, for spike-free operation the input data transitions should occur as soon as possible after the triggering edge.

The CARRY is reset to a logical "0" at the end of each word by applying a logical "1" signal to a CARRY-RESET input one-bit-position before the application of the first bit of the next word.

The CD4032B and CD4038B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4032B, CD4038B
FUNCTIONAL DIAGRAM

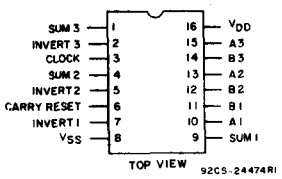
Features:

- Invert inputs on all adders for sum complementing applications
- Fully static operation . . . . dc to 10 MHz (typ.) @ V_{DD} = 10 V
- Single-phase clocking
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range)
  - 1 V at V_{DD} = 5 V
  - 2 V at V_{DD} = 10 V
  - 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Serial arithmetic units
- Digital correlators
- Digital datalink computers
- Flight control computers
- Digital servo control systems

CD4032B, CD4038B
TERMINAL DIAGRAM



MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) ..... −0.5 to +20 V
(Voltages referenced to V_{SS} Terminal)
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H ..... −55 to +125°C
PACKAGE TYPE E ..... −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC		V_{DD}	Min.	Max.	UNITS
Supply Voltage Range (at T_A = Full Package-Temperature Range)			3	18	V
Clock Input Frequency,	f_{CL}	5	–	2.5	MHz
		10	–	5	
		15	–	7.5	
Clock Input Rise or Fall Time,	t_rCL, t_fCL	5	–	500	μs
		10	–	500	
		15	–	500	
Data Input Set-Up Time, Clock to A or B Inputs	t_{SU}	5	200	–	ns
		10	80	–	
		15	60		

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, K, H, Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

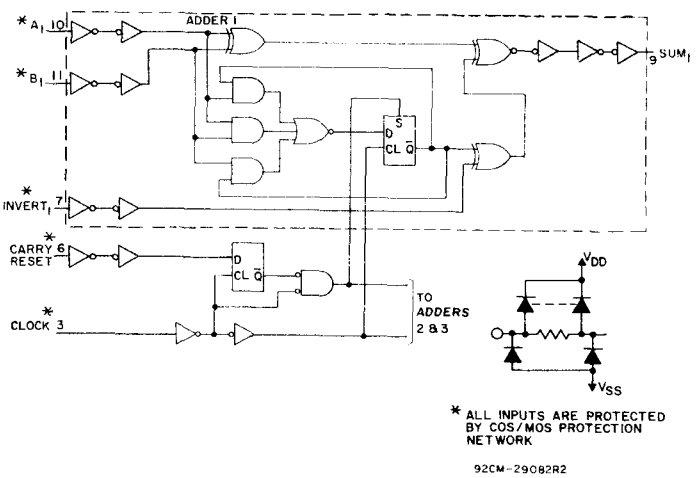


Fig.1 – CD4032B logic diagram of one of three serial adders.

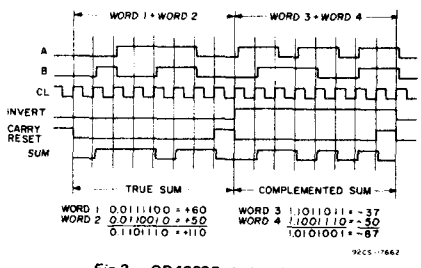


Fig.2 – CD4032B timing diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25°C$, Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ*

CHARACTERISTIC	TEST CONDITIONS V_{DD}(V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} A,B, Carry Reset, or Invert Inputs to Sum Outputs	5	–	260	520	ns
	10	–	120	240	
	15	–	90	180	
Clock Input to Sum Outputs	5	–	325	650	ns
	10	–	175	350	
	15	–	150	300	
Transition Time: t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Minimum Data Input Setup Time, t_{SU} Clock to A or B Inputs	5	–	125	200	ns
	10	–	50	80	
	15	–	40	60	
Maximum Clock Input Frequency, f_{CL}	5	2.5	4.5	–	MHz
	10	5	10	–	
	15	7.5	15	–	
Clock Input Rise or Fall Time, t_{rCL},t_{fCL}*	5	–	–	500	μs
	10	–	–	500	
	15	–	–	500	
Input Capacitance, C_{IN}	(Any Input)	–	5	7.5	pF

* If more than one unit is cascaded t_{rCL} should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

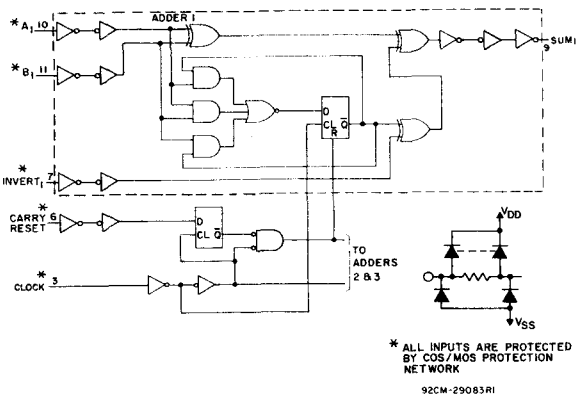


Fig. 3 – CD4038B logic diagram of one of three serial adders.

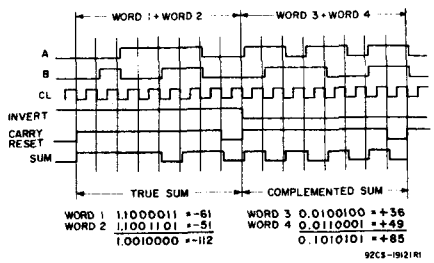


Fig.4 – CD4038B timing diagram.

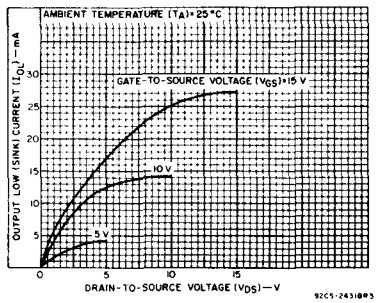


Fig. 5 – Typical output low (sink) current characteristics.

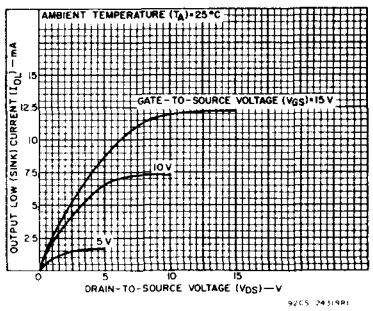


Fig. 6 – Minimum output low (sink) current characteristics.

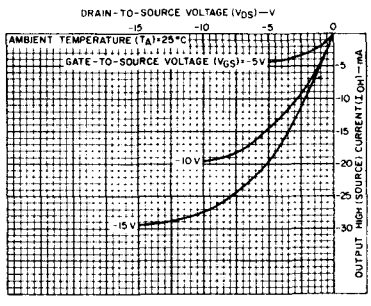


Fig. 7 – Typical output high (source) current characteristics.

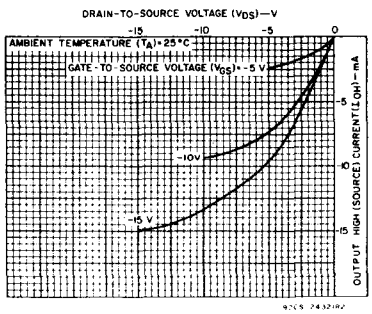


Fig. 8 – Minimum output high (source) current characteristics.

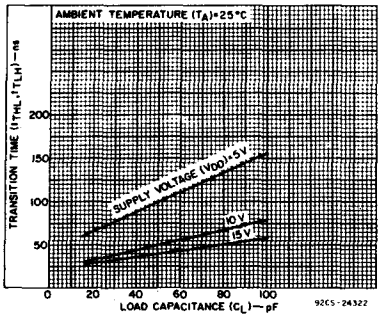


Fig. 9 – Typical transition time as a function of load capacitance.

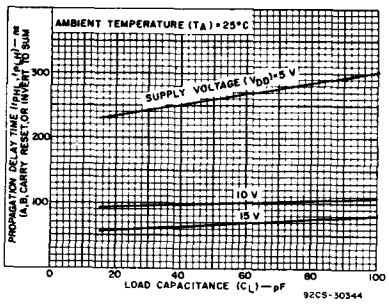


Fig. 10 – Typical propagation delay times as a function of load capacitance (A, B, carry reset or invert to SUM).

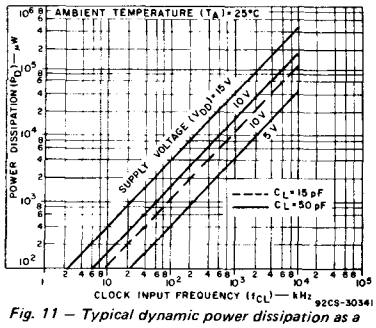


Fig. 11 – Typical dynamic power dissipation as a function of clock input frequency.

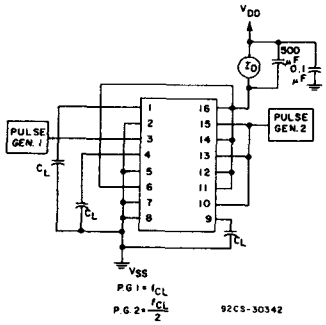


Fig. 12 – Dynamic power dissipation test circuit.

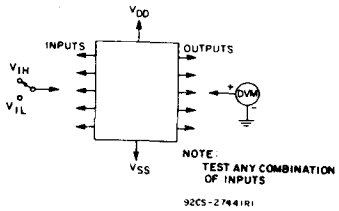


Fig. 13 – Input voltage test circuit.

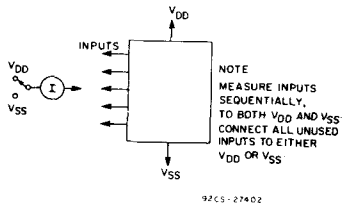


Fig. 14 – Input current test circuit.

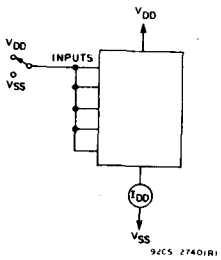
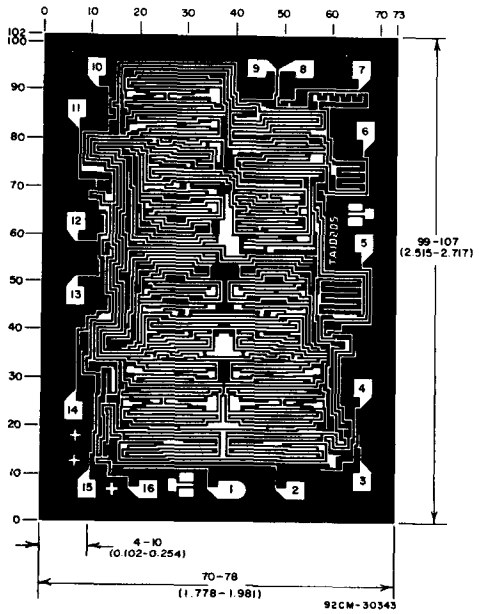


Fig. 15 – Quiescent-device current test circuit.



Dimensions and pad layout for CD4032BH; dimensions and pad layout for CD4038BH are identical.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.