

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4018B

MSI

Presetable divide-by-N counter

Product specification
File under Integrated Circuits, IC04

January 1995

Presettable divide-by-N counter

HEF4018B
MSI

PRESETTABLE DIVIDE-BY-N COUNTER

The HEF4018B is a 5-stage Johnson counter with a clock input (CP), a data input (D), an asynchronous parallel load input (PL), five parallel inputs (P₀ to P₄), five active LOW buffered outputs (\bar{O}_0 to \bar{O}_4), and an overriding asynchronous master reset input (MR). Information on P₀ to P₄ is asynchronously loaded into the counter while PL is HIGH, independent of CP and D inputs. When P_L is LOW, the counter advances on the LOW to HIGH transition of CP. By connecting \bar{O}_0 to \bar{O}_4 to D, the counter operates as a divide-by-n counter (n = 2 to 10; see also function selection below). Each register stage is a D-type master-slave flip-flop with a set-direct/clear-direct input. An internal code correction circuit provides automatic code correction of the counter. From any illegal code the counter is in a proper counting mode within 11 clock pulses. A HIGH on MR resets the counter (\bar{O}_0 to \bar{O}_4 = HIGH) independent of all other inputs.

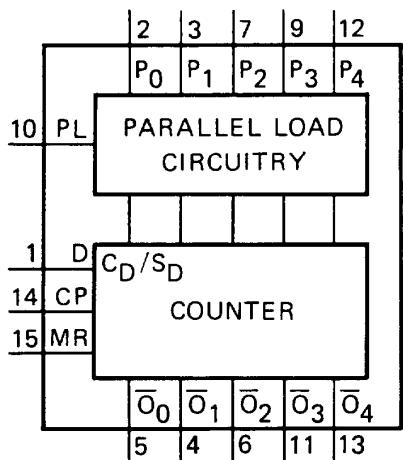


Fig. 1 Functional diagram.

FUNCTION SELECTION

counter mode; divide by	connect D input to	remarks
10 8 6 4 2	\bar{O}_4 \bar{O}_3 \bar{O}_2 \bar{O}_1 \bar{O}_0	no external components needed
9 7 5 3	$\bar{O}_3 \cdot \bar{O}_4$ $\bar{O}_2 \cdot \bar{O}_3$ $\bar{O}_1 \cdot \bar{O}_2$ $\bar{O}_0 \cdot \bar{O}_1$	AND gate needed; counter skips all HIGH states

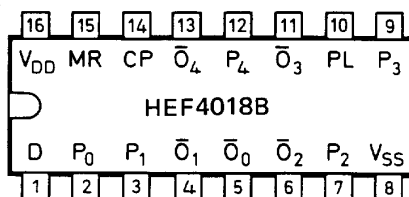


Fig. 2 Pinning diagram.

- HEF4018BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4018BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4018BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

- PL parallel load input
- P₀ to P₄ parallel inputs
- D data input
- CP clock input (LOW to HIGH edge triggered)
- MR master reset input
- \bar{O}_0 to \bar{O}_4 buffered output (active LOW)

APPLICATION INFORMATION

Some examples of applications for the HEF4018B are:

- Programmable divide-by-n counter
- Programmable frequency division
- Timers

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

Pre-settable divide-by-N counter

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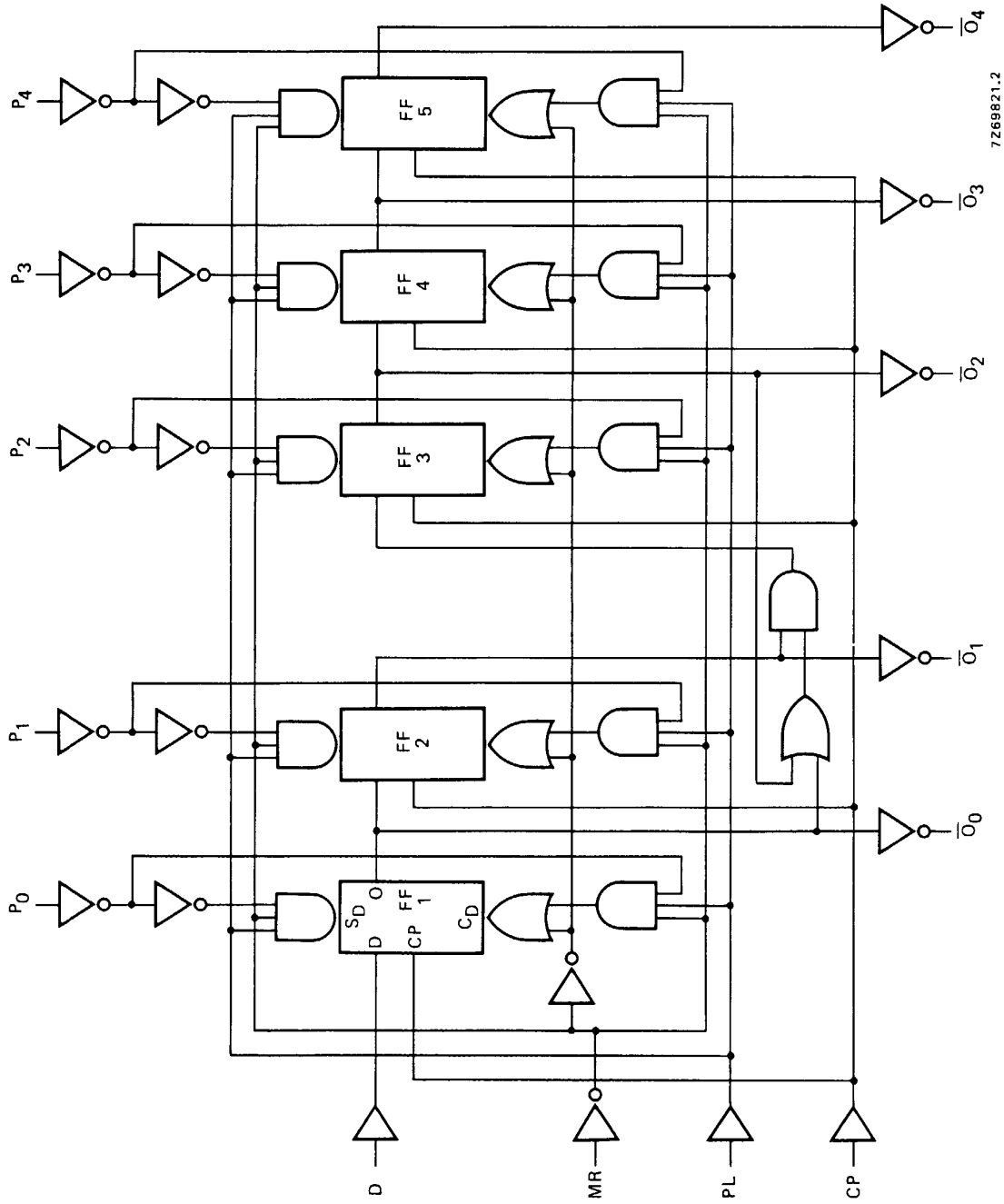


Fig. 3 Logic diagram.

Presettable divide-by-N counter

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A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$3450 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$10\,300 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula		
Propagation delays CP \rightarrow \bar{O} HIGH to LOW	5	t_{PHL}		185	370	ns	$158\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		65	135	ns	$54\text{ ns} + (0,23\text{ ns/pF}) C_L$		
	15		50	95	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$		
	LOW to HIGH	5	t_{PLH}		145	295	ns	$118\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		55	110	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$	
		15		40	85	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
PL \rightarrow \bar{O} HIGH to LOW	5	t_{PHL}		205	415	ns	$178\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		70	140	ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$		
	15		50	105	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$		
	LOW to HIGH	5	t_{PLH}		175	350	ns	$148\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		65	125	ns	$54\text{ ns} + (0,23\text{ ns/pF}) C_L$	
		15		50	95	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$	
MR \rightarrow \bar{O} LOW to HIGH	5	t_{PLH}		140	280	ns	$113\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		55	105	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$		
	15		40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$		
	Output transition times	5	t_{THL}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
		10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
		15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
LOW to HIGH		5	t_{TLH}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
		10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
		15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	

Pre-settable divide-by-N counter

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A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Set-up time D \rightarrow CP	5	t_{su}	130	65	ns	see also waveforms Figs 4, 5 and 6
	10		40	20	ns	
	15		30	15	ns	
Hold time D \rightarrow CP	5	t_{hold}	20	-45	ns	
	10		5	-15	ns	
	15		5	-10	ns	
Minimum clock pulse width; LOW	5	t_{WCPL}	140	70	ns	
	10		50	25	ns	
	15		40	20	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	100	50	ns	
	10		35	20	ns	
	15		25	15	ns	
Minimum PL pulse width; HIGH	5	t_{WPLH}	145	75	ns	
	10		50	25	ns	
	15		35	20	ns	
Recovery time for MR	5	t_{RMR}	135	70	ns	
	10		40	20	ns	
	15		25	15	ns	
Recovery time for PL	5	t_{RPL}	170	85	ns	
	10		55	30	ns	
	15		40	20	ns	
Maximum clock pulse frequency	5	f_{max}	2	4	MHz	
	10		6	11	MHz	
	15		8	16	MHz	

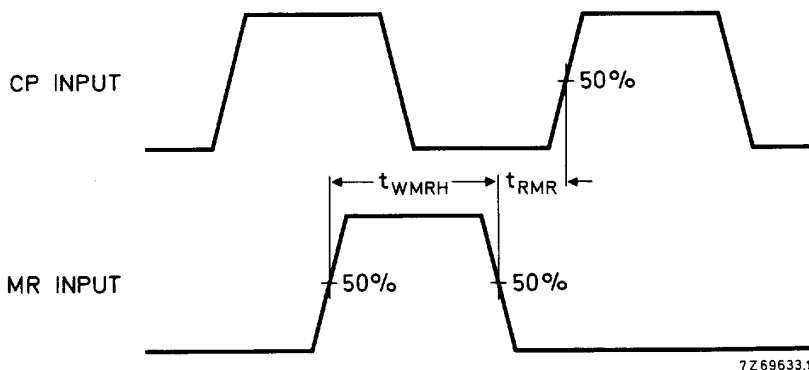


Fig. 4 Waveforms showing minimum MR pulse width and MR recovery time.

Pre-settable divide-by-N counter

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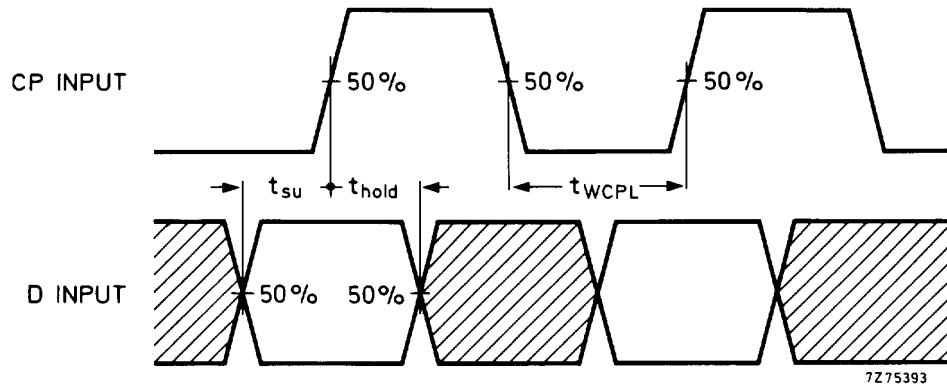


Fig. 5 Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D.

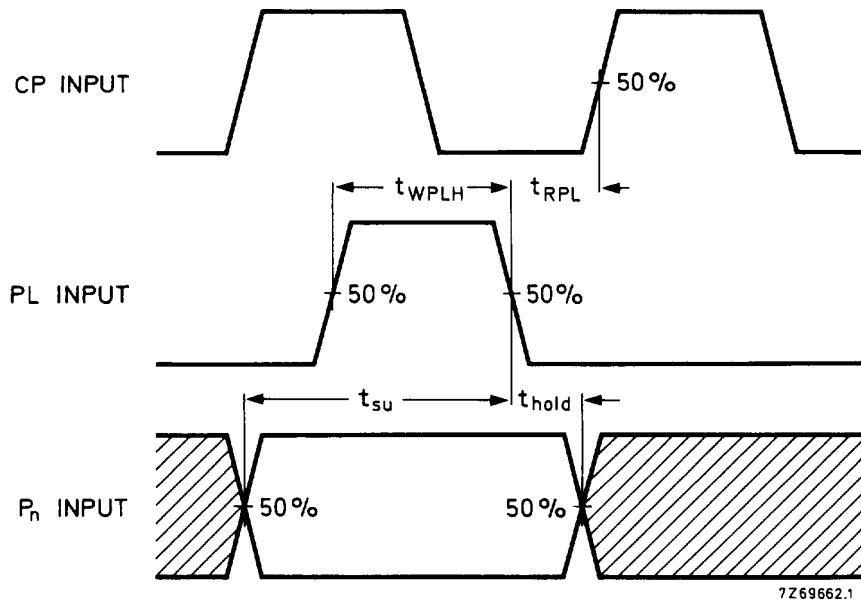


Fig. 6 Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for P_n to PL. Set-up and hold times are shown as positive values but may be specified as negative values.

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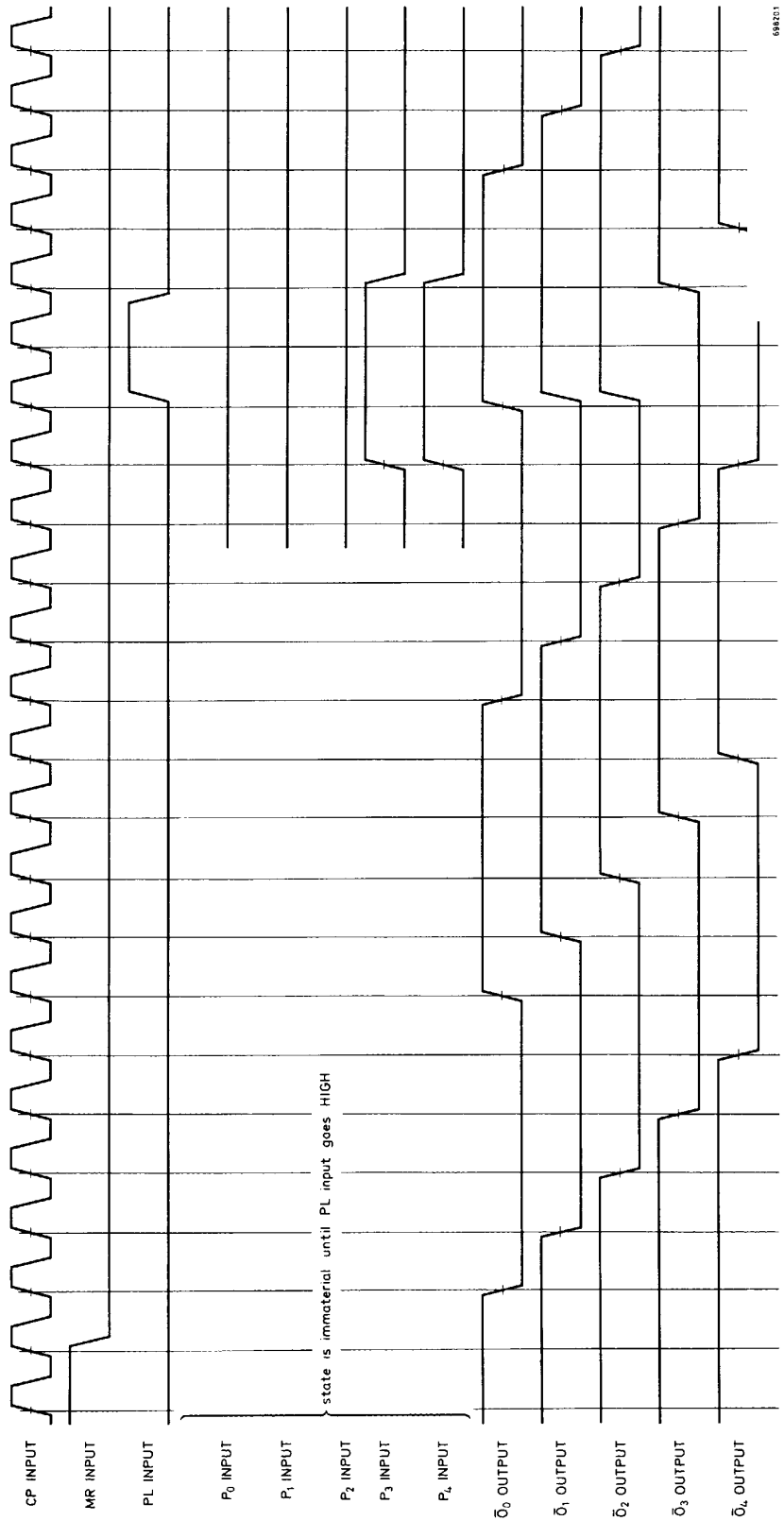
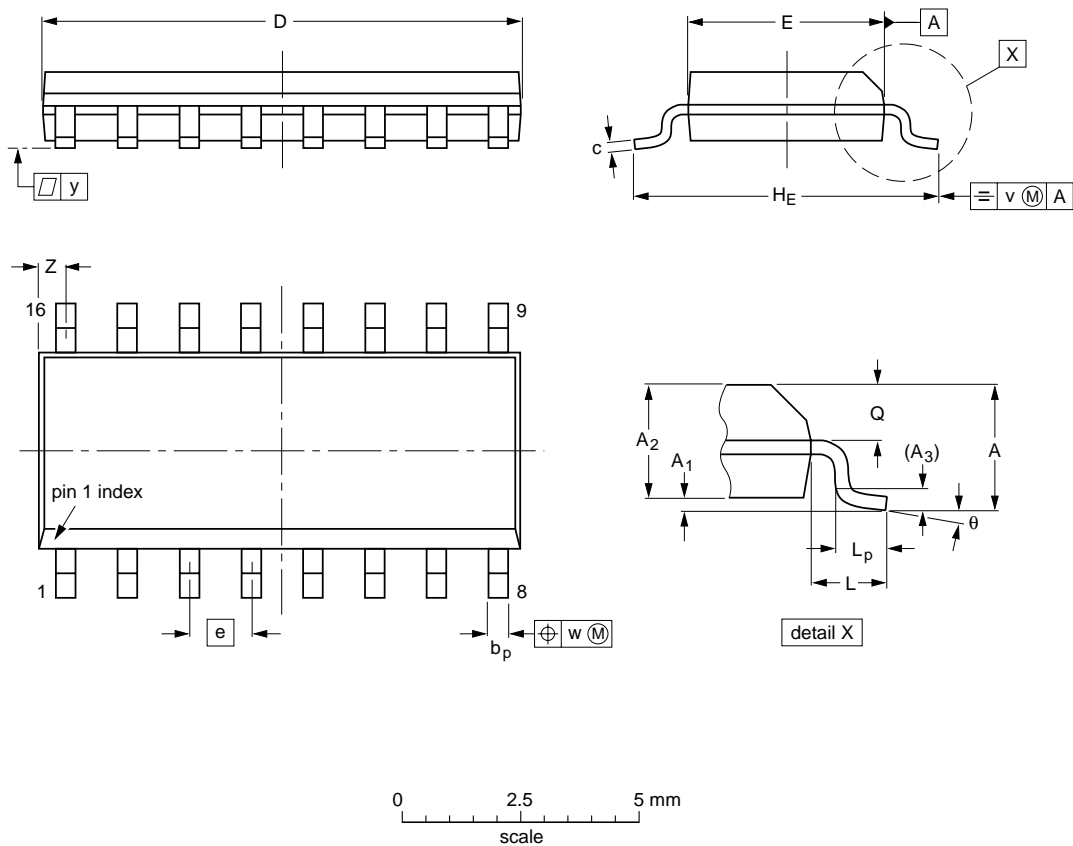


Fig. 7 Timing diagram.

Note
D input connected to \bar{Q}_4 for decade counter configuration.

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

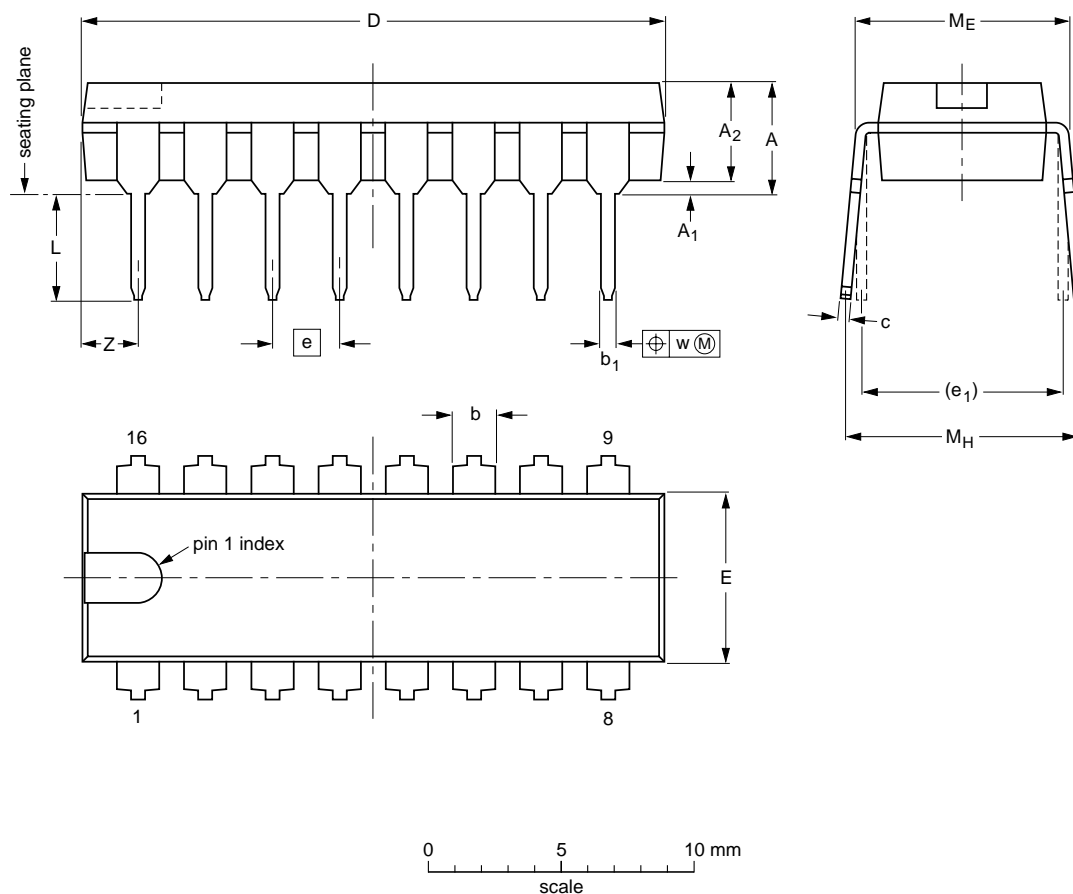
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				92-10-02 95-01-19