

# HEF4013B

## Dual D-type flip-flop

Rev. 8 — 21 November 2011

Product data sheet

## 1. General description

The HEF4013B is a dual D-type flip-flop that features independent set-direct input (SD), clear-direct input (CD), clock input (CP) and outputs (Q,  $\bar{Q}$ ). Data is accepted when CP is LOW and is transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous CD and SD inputs are independent and override the D or CP inputs. The outputs are buffered for best system performance. The clock input's Schmitt-trigger action makes the circuit highly tolerant of slower clock rise and fall times.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

## 2. Features and benefits

- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

## 3. Applications

- Counters and dividers
- Registers
- Toggle flip-flops

## 4. Ordering information

**Table 1. Ordering information**

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

Type number	Package		Version
	Name	Description	
HEF4013BP	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
HEF4013BT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
HEF4013BTT	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1



5. Functional diagram

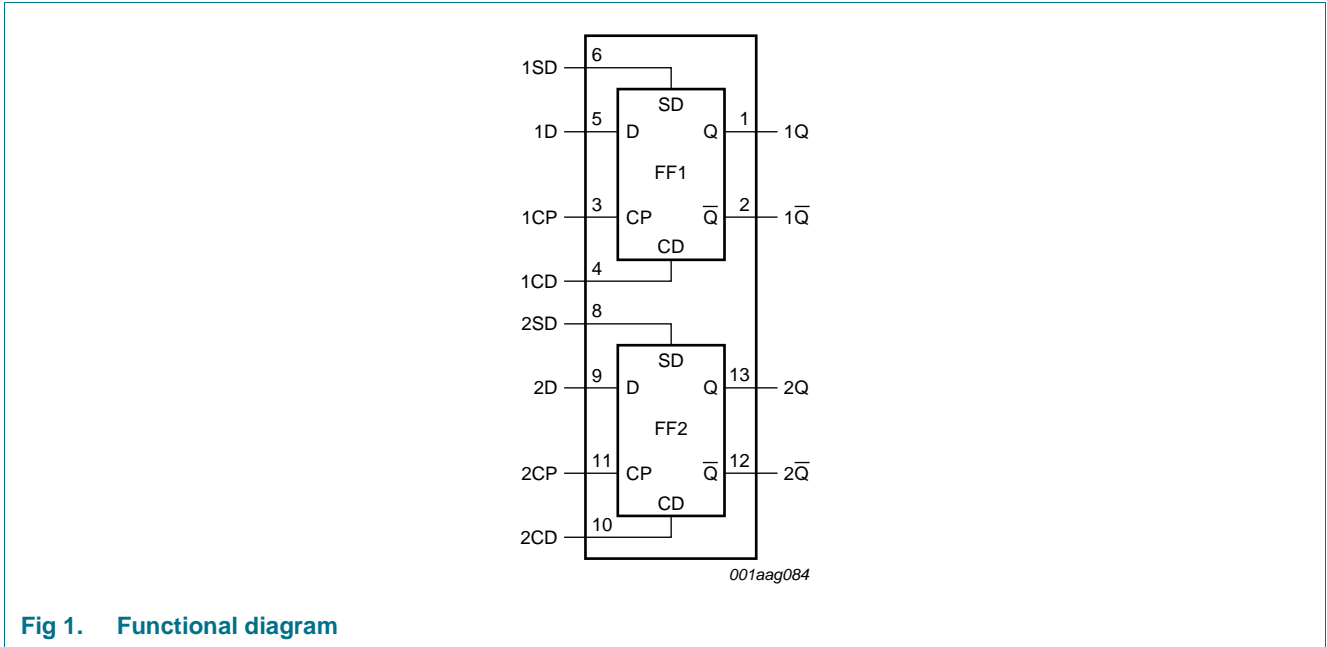


Fig 1. Functional diagram

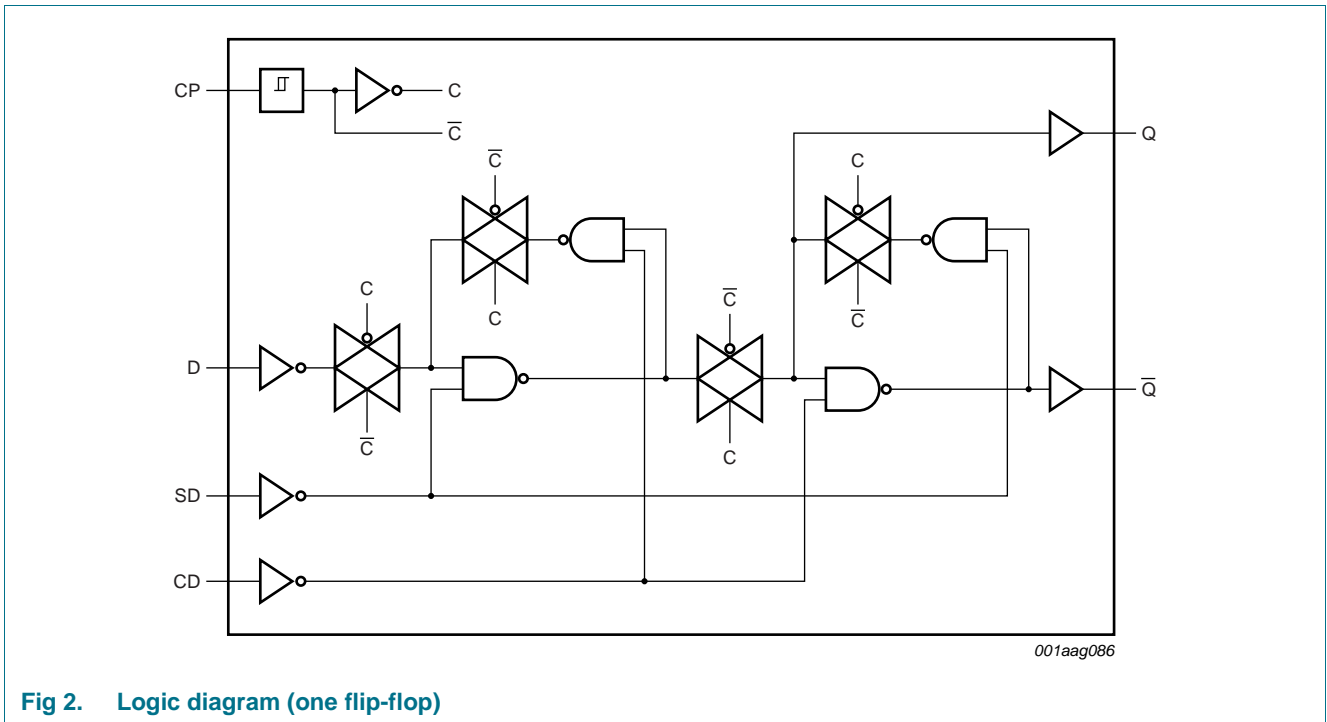


Fig 2. Logic diagram (one flip-flop)

## 6. Pinning information

### 6.1 Pinning

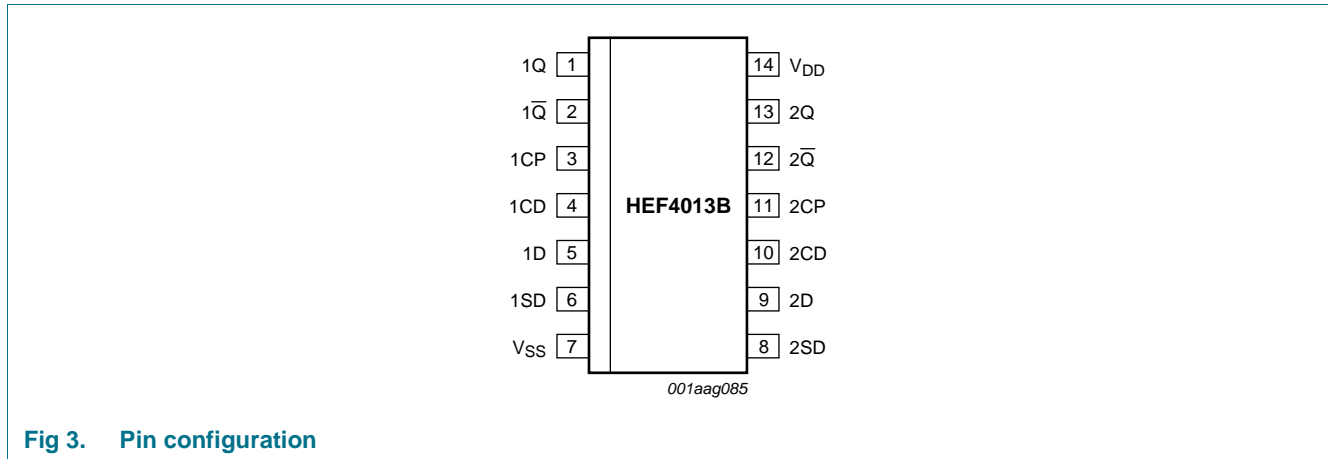


Fig 3. Pin configuration

### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1Q, 2Q	1, 13	true output
1Q̄, 2Q̄	2, 12	complement output
1CP, 2CP	3, 11	clock input (LOW to HIGH edge-triggered)
1CD, 2CD	4, 10	asynchronous clear-direct input (active HIGH)
1D, 2D	5, 9	data input
1SD, 2SD	6, 8	asynchronous set-direct input (active HIGH)
V <sub>SS</sub>	7	ground (0 V)
V <sub>DD</sub>	14	supply voltage

## 7. Functional description

Table 3. Function table<sup>[1]</sup>

Control			Input	Output	
nSD	nCD	nCP	nD	nQ	nQ̄
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H
L	L	↑	L	L	H
L	L	↑	H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition.

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to  $V_{SS} = 0$  V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V	-	$\pm 10$	mA
$I_{I/O}$	input/output current		-	$\pm 10$	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+125	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
		DIP14	[1] -	750	mW
		SO14	[2] -	500	mW
		TSSOP14	[3] -	500	mW
P	power dissipation	per output	-	100	mW

[1] For DIP14 packages: above  $T_{amb} = 70$  °C,  $P_{tot}$  derates linearly with 12 mW/K.

[2] For SO14 packages: above  $T_{amb} = 70$  °C,  $P_{tot}$  derates linearly with 8 mW/K.

[3] For TSSOP14 packages: above  $T_{amb} = 60$  °C,  $P_{tot}$  derates linearly with 5.5 mW/K.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		3	15	V
$V_I$	input voltage		0	$V_{DD}$	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5$ V	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10$ V	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15$ V	-	0.08	$\mu\text{s/V}$

## 10. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		$T_{amb} = +125\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.1$	-	$\pm 0.1$	-	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	all valid input combinations; $ I_O  = 0\text{ A}$	5 V	-	1.0	-	1.0	-	30	-	30	$\mu\text{A}$
			10 V	-	2.0	-	2.0	-	60	-	60	$\mu\text{A}$
			15 V	-	4.0	-	4.0	-	120	-	120	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	7.5	-	-	-	-	pF	

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified. For test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula	Min	Typ	Max	Unit
t <sub>PHL</sub>	HIGH to LOW propagation delay	nCP to nQ, n $\bar{Q}$ ; see <a href="#">Figure 4</a>	5 V	<a href="#">[1]</a> $83 + 0.55 \times C_L$	-	110	220	ns
			10 V	$34 + 0.23 \times C_L$	-	45	90	ns
			15 V	$22 + 0.16 \times C_L$	-	30	60	ns
		nSD to n $\bar{Q}$	5 V	<a href="#">[1]</a> $73 + 0.55 \times C_L$	-	100	200	ns
			10 V	$29 + 0.23 \times C_L$	-	40	80	ns
			15 V	$22 + 0.16 \times C_L$	-	30	60	ns
		nCD to nQ	5 V	<a href="#">[1]</a> $73 + 0.55 \times C_L$	-	100	200	ns
			10 V	$29 + 0.23 \times C_L$	-	40	80	ns
			15 V	$22 + 0.16 \times C_L$	-	30	60	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	nCP to nQ, n $\bar{Q}$ ; see <a href="#">Figure 4</a>	5 V	<a href="#">[1]</a> $68 + 0.55 \times C_L$	-	95	190	ns
			10 V	$29 + 0.23 \times C_L$	-	40	80	ns
			15 V	$22 + 0.16 \times C_L$	-	30	60	ns
		nSD to nQ	5 V	<a href="#">[1]</a> $48 + 0.55 \times C_L$	-	75	150	ns
			10 V	$24 + 0.23 \times C_L$	-	35	70	ns
			15 V	$17 + 0.16 \times C_L$	-	25	50	ns
		nCD to n $\bar{Q}$	5 V	<a href="#">[1]</a> $33 + 0.55 \times C_L$	-	60	120	ns
			10 V	$19 + 0.23 \times C_L$	-	30	60	ns
			15 V	$12 + 0.16 \times C_L$	-	20	40	ns
t <sub>t</sub>	transition time	see <a href="#">Figure 4</a>	5 V	<a href="#">[1]</a> $10 + 1.00 \times C_L$	-	60	120	ns
			10 V	$9 + 0.42 \times C_L$	-	30	60	ns
			15 V	$6 + 0.28 \times C_L$	-	20	40	ns
t <sub>su</sub>	set-up time	nD to nCP; see <a href="#">Figure 4</a>	5 V		40	20	-	ns
			10 V		25	10	-	ns
			15 V		15	5	-	ns
t <sub>h</sub>	hold time	nD to nCP; see <a href="#">Figure 4</a>	5 V		20	0	-	ns
			10 V		20	0	-	ns
			15 V		15	0	-	ns
t <sub>w</sub>	pulse width	nCP input LOW; see <a href="#">Figure 4</a>	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		nSD input HIGH; see <a href="#">Figure 5</a>	5 V		50	25	-	ns
			10 V		24	12	-	ns
			15 V		20	10	-	ns
		nCD input HIGH; see <a href="#">Figure 5</a>	5 V		50	25	-	ns
			10 V		24	12	-	ns
			15 V		20	10	-	ns

**Table 7. Dynamic characteristics ...continued**  
 $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified. For test circuit see [Figure 6](#).

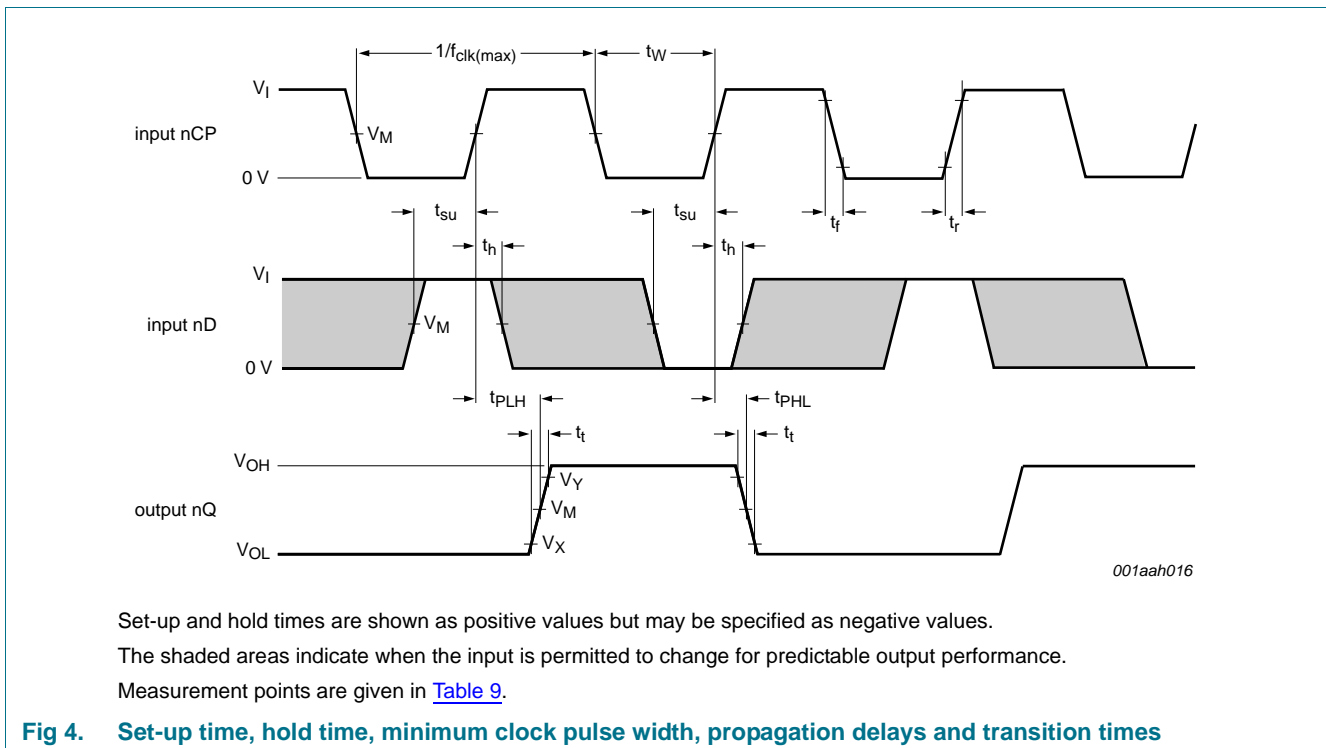
Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula	Min	Typ	Max	Unit
$t_{rec}$	recovery time	nSD input; see <a href="#">Figure 5</a>	5 V		+15	-5	-	ns
			10 V		15	0	-	ns
			15 V		15	0	-	ns
		nCD input; see <a href="#">Figure 5</a>	5 V		40	25	-	ns
			10 V		25	10	-	ns
			15 V		25	10	-	ns
$f_{clk(max)}$	maximum clock frequency	see <a href="#">Figure 4</a>	5 V		7	14	-	MHz
			10 V		14	28	-	MHz
			15 V		20	40	-	MHz

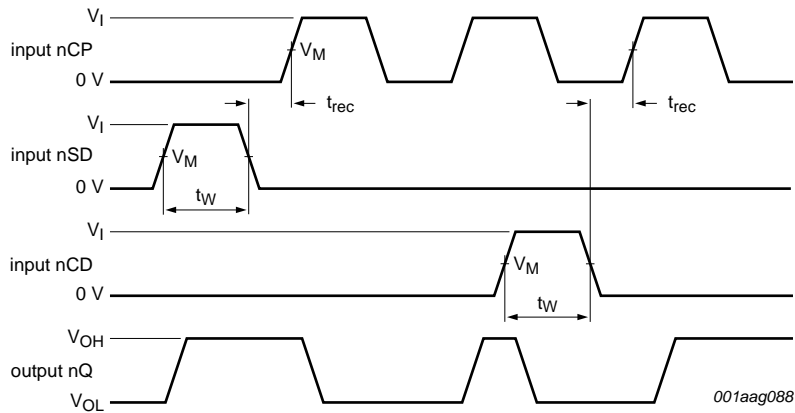
[1] Typical values of the propagation delays and output transition times can be calculated with the extrapolation formulas.  $C_L$  is given in pF.

**Table 8. Dynamic power dissipation**  
 $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	$V_{DD}$	Typical formula	Where
$P_D$	dynamic power dissipation	5 V	$P_D = 850 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\text{ }\mu\text{W}$	$f_i$ = input frequency in MHz;
		10 V	$P_D = 3600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\text{ }\mu\text{W}$	$f_o$ = output frequency in MHz;
		15 V	$P_D = 9000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\text{ }\mu\text{W}$	$C_L$ = output load capacitance in pF; $\Sigma(f_o \times C_L)$ = sum of the outputs; $V_{DD}$ = supply voltage in V.

## 12. Waveforms



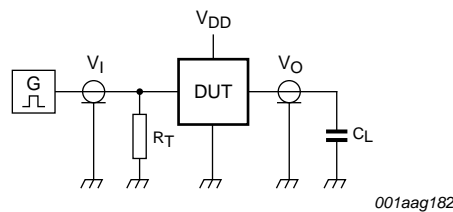


Recovery times are shown as positive values but may be specified as negative values.  
Measurement points are given in [Table 9](#).

**Fig 5. nSD, nCD recovery time and pulse width**

**Table 9. Measurement points**

Supply voltage	Input	Output		
$V_{DD}$	$V_M$	$V_M$	$V_X$	$V_Y$
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$	$0.1V_{DD}$	$0.9V_{DD}$



Test and measurement data is given in [Table 10](#);

Definitions test circuit:

DUT = Device Under Test.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

**Fig 6. Test circuit for measuring switching times**

**Table 10. Test data**

Supply voltage	Input	Load	
$V_{DD}$	$V_I$	$t_r, t_f$	$C_L$
5 V to 15 V	$V_{SS}$ or $V_{DD}$	$\leq 20$ ns	50 pF



### 13. Application information

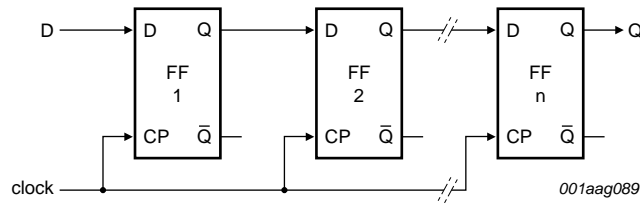


Fig 7. N-stage shift register

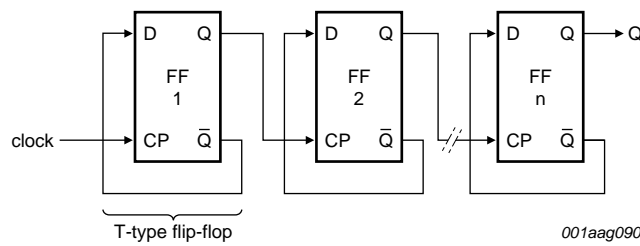


Fig 8. Binary ripple up-counter; divide-by- $2^n$

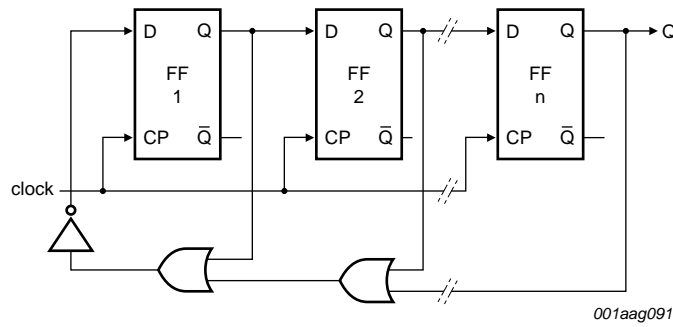


Fig 9. Modified ring counter; divide-by-( $n + 1$ )

14. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

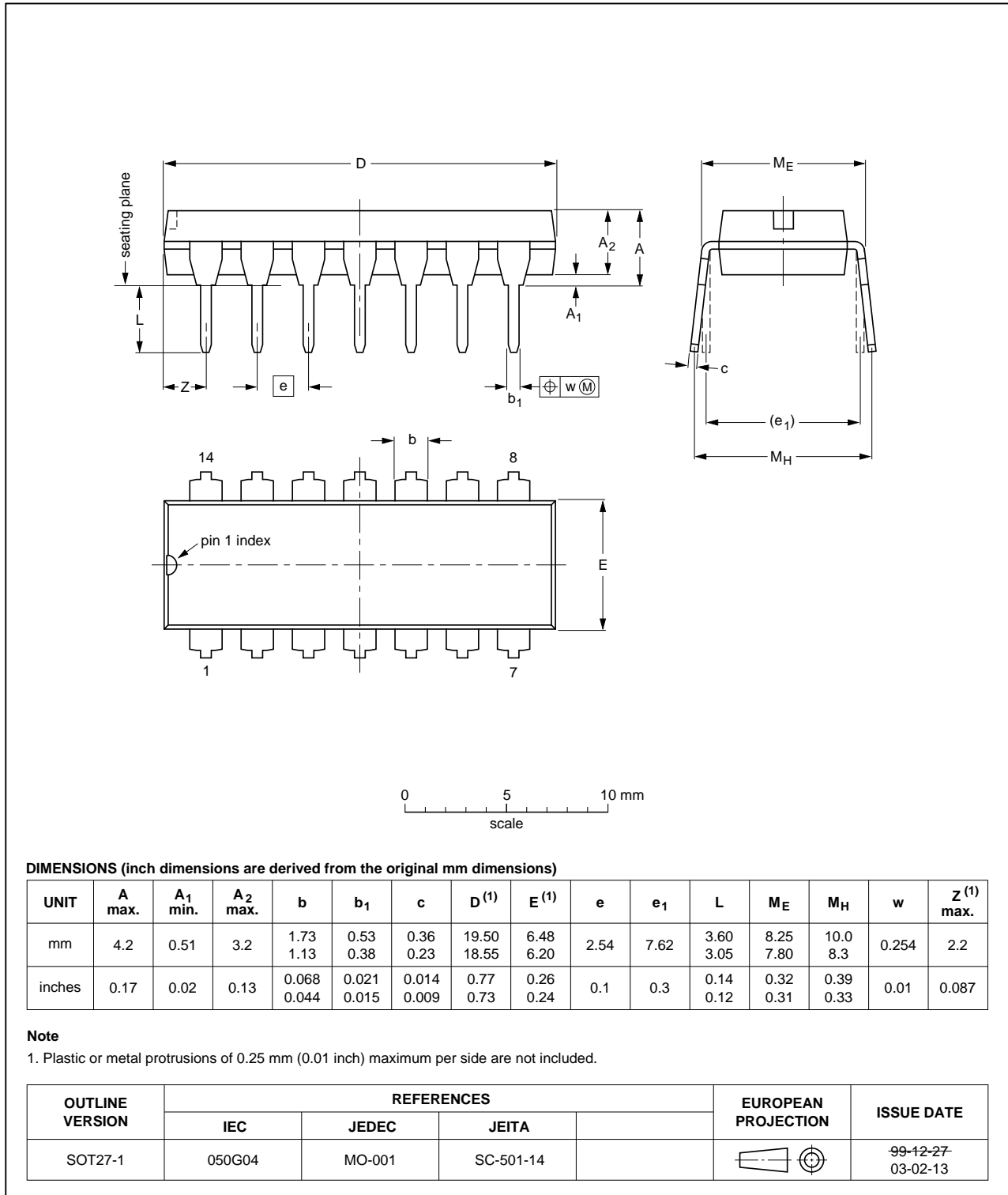


Fig 10. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

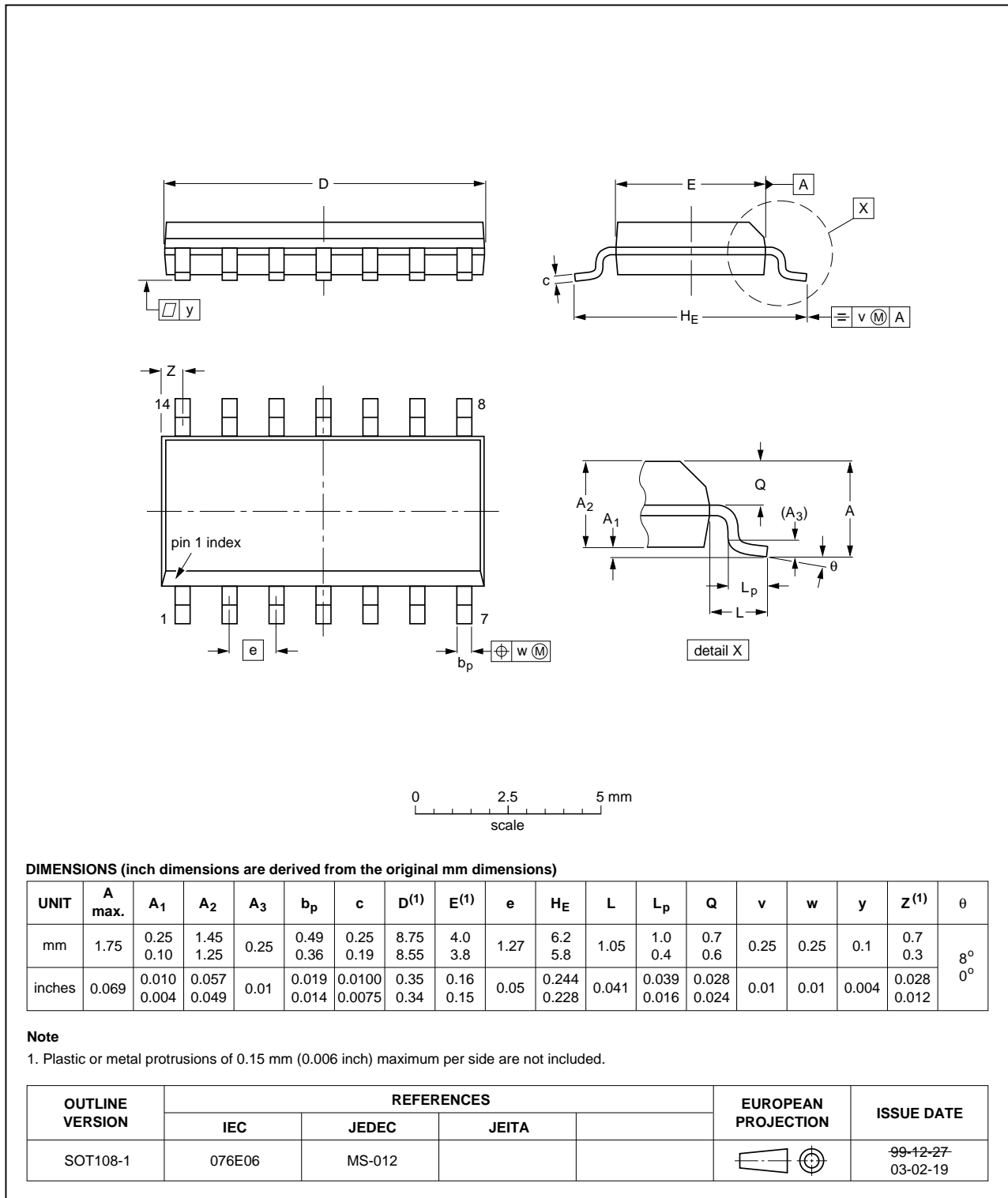


Fig 11. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

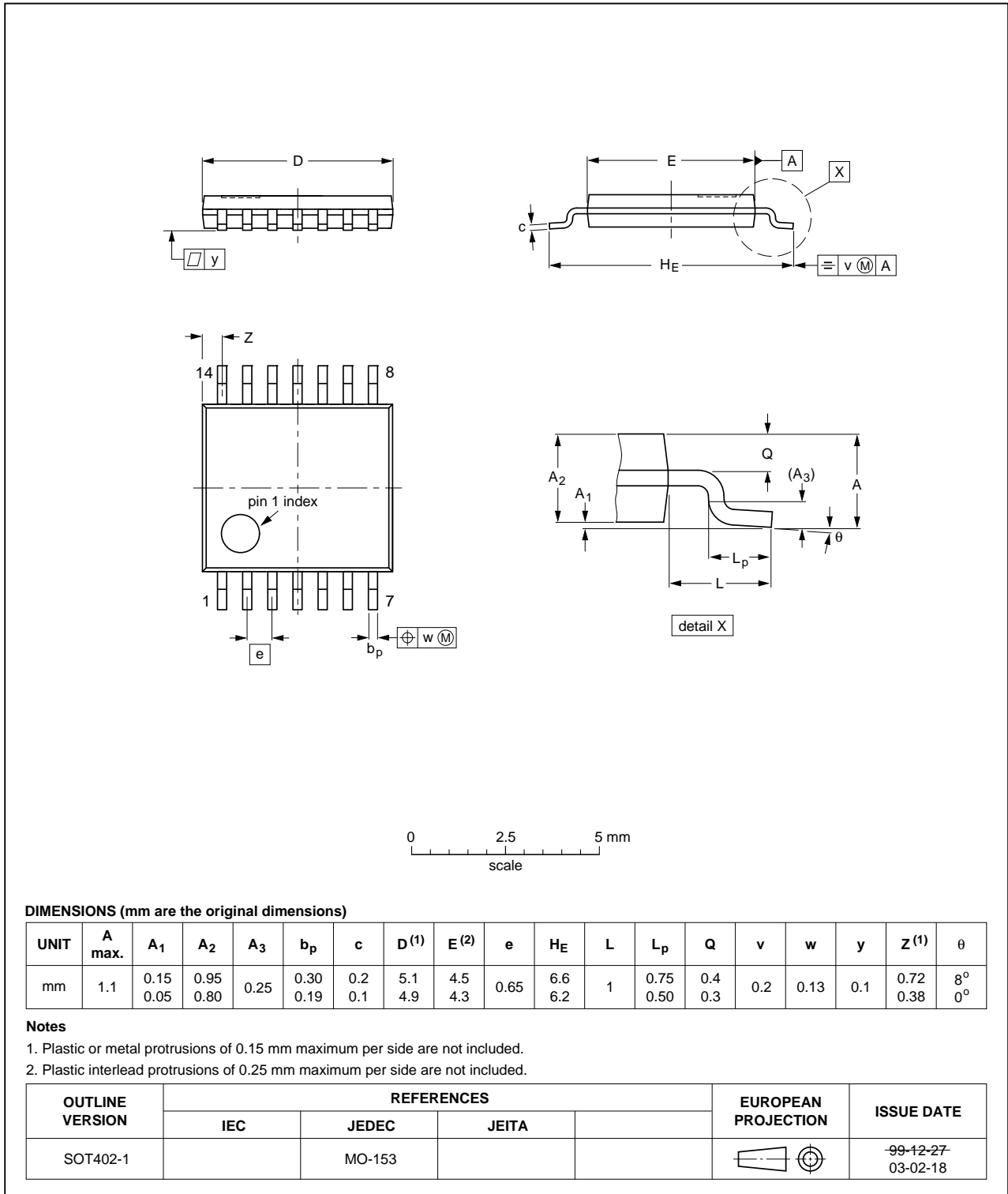


Fig 12. Package outline SOT402-1 (TSSOP14)

## 15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4013B v.8	20111121	Product data sheet	-	HEF4013B v.7
Modifications:		<ul style="list-style-type: none"><li>• Legal pages updated.</li><li>• Changes in “General description”, “Features and benefits” and “Applications”.</li></ul>		
HEF4013B v.7	20110913	Product data sheet	-	HEF4013B v.6
HEF4013B v.6	20091027	Product data sheet	-	HEF4013B v.5
HEF4013B v.5	20090619	Product data sheet	-	HEF4013B v.4
HEF4013B v.4	20080515	Product data sheet	-	HEF4013B_CNV v.3
HEF4013B_CNV v.3	19950101	Product specification	-	HEF4013B_CNV v.2
HEF4013B_CNV v.2	19950101	Product specification	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 16.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 16.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

## 16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 18. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Applications</b> .....	<b>1</b>
<b>4</b>	<b>Ordering information</b> .....	<b>1</b>
<b>5</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>6</b>	<b>Pinning information</b> .....	<b>3</b>
6.1	Pinning .....	3
6.2	Pin description .....	3
<b>7</b>	<b>Functional description</b> .....	<b>3</b>
<b>8</b>	<b>Limiting values</b> .....	<b>4</b>
<b>9</b>	<b>Recommended operating conditions</b> .....	<b>4</b>
<b>10</b>	<b>Static characteristics</b> .....	<b>5</b>
<b>11</b>	<b>Dynamic characteristics</b> .....	<b>6</b>
<b>12</b>	<b>Waveforms</b> .....	<b>7</b>
<b>13</b>	<b>Application information</b> .....	<b>9</b>
<b>14</b>	<b>Package outline</b> .....	<b>10</b>
<b>15</b>	<b>Revision history</b> .....	<b>13</b>
<b>16</b>	<b>Legal information</b> .....	<b>14</b>
16.1	Data sheet status .....	14
16.2	Definitions .....	14
16.3	Disclaimers .....	14
16.4	Trademarks .....	15
<b>17</b>	<b>Contact information</b> .....	<b>15</b>
<b>18</b>	<b>Contents</b> .....	<b>16</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 21 November 2011

Document identifier: HEF4013B