74LS429
FIFO RAM Controller (FRC)

Preliminary Specification

Logic Products

FEATURES

- **Direct addressing up to 64K**
- **Cascadable for addressing beyond 64K**
- **Asynchronous Read/Write operation**
- **3-State address outputs**
- **Selectable FIFO length in multiples of 2**
- **Specially designed for use with high-speed SRAMs**
- **TTL input and output**
- **16mA address-drive capability**
- **Programmable half-full signal**
- **Programmable Read, Write and Status counters**

DESCRIPTION

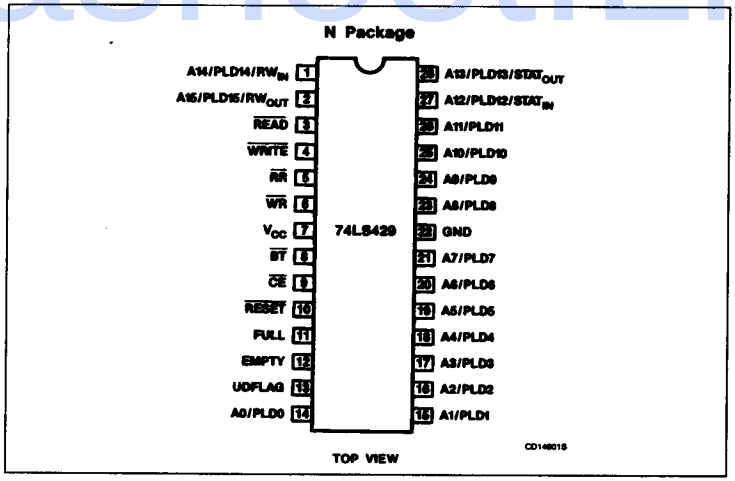
The FRC is an address and status generator designed to implement high-speed/high-capacity First-In First-Out (FIFO) memory buffers utilizing high-speed SRAMs. The FRC can control up to 65,536 (64K) words of buffer memory. The Address Length Register and the Read, Write, and Status Counters are fully programmable. There is also a user-definable status flag to aid in block transfers. The device is cascadable if FIFO buffers in excess of 64K are desired. In the cascade mode, two devices can address up to 16 Mega-words of memory.

TYPE	TYPICAL TRANSFER RATE	TYPICAL SUPPLY CURRENT
74LS429	20MHz	185mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ± 5%, T_A = 0°C to +70°C
28-Pin Plastic DIP	N74LS429N

PIN CONFIGURATION



ARCHITECTURE

The FRC (Figure 1) is made up of three 16-bit counters, arbitration logic, mux/latch circuitry and the necessary control logic to generate status flags and control the device. Two of the counters (Read and Write) are up counters and are used to generate addresses for the memory. The third counter (Status) is an up/down counter and is used to generate the status flags, i.e, FULL, EMPTY and User-Defined Flag (UDFLAG).

The Read ($\overline{RR}$) and Write ($\overline{WR}$) requests may occur asynchronously, but only one operation (either Read or Write) will be serviced by the FRC. This decision is made by the arbitration logic.

In the normal mode the device has a maximum of 16 address outputs. A Write request will cause the contents of the Write Counter to be transferred to these outputs and the $\overline{WRITE}$ output to go Low. After the request is removed the Write and Status counters will be updated so that they will be ready when the next Write request occurs. A Read request will cause the contents of the Read Counter to be transferred to the address outputs and the $\overline{READ}$ output to go Low. After the request is removed, Read and Status counters are updated. The device may also be used in cascade mode. When used in this way the most significant four-address outputs (A12 – A15) are no longer address outputs but are used instead for transferring the conditions of the three internal counters from one device to the next. Two devices cascaded will have a combined address length of 24-bits which can address 16 mega-words of memory.

The Burst Transfer Mode allows the device to be exclusively used as either a Write address or Read address generator by disabling the complementary operation (Read or Write). An example of when this mode might be used is the case where a fast processor and a slow peripheral are both accessing the FIFO buffer at the same time. The processor could block the peripheral from accessing the FIFO by forcing the Burst Transfer ($\overline{BT}$) input Low (while it is making a request) and then continue reading or writing without having to interleave cycles with the slower peripheral. When the processor completes its operation, it will force the $\overline{BT}$ input High, allowing the peripheral to access the FIFO.

The two internal registers (Address Length and UDFLAG) and the three counters (Read, Write, and Status) are fully programmable.

The control logic automatically compensates for address lengths less than 16 bits (per device); therefore, the status flags (FULL, EMPTY, and UDFLAG) are always generated to reflect the appropriate condition.

PIN DESCRIPTION

PIN NO.	SYMBOL	TYPE	DESCRIPTION
5	$\overline{RR}$	I	**READ REQUEST** for Read cycle: A High-to-Low transition causes the contents of the Read Counter to be transferred to the address outputs followed by assertion of the $\overline{READ}$ output. The Read and Status Counters are incremented and decremented respectively on the Low-to-High transition. $\overline{READ}$ output is also negated at this time, but the address bus is held in the stable state. This input is used as a control pin when presetting the internal counters and registers (see Table 1).
6	$\overline{WR}$	I	**WRITE REQUEST** for Write cycle: A High-to-Low transition causes the contents of the Write Counter to be transferred to the address outputs followed by assertion of the $\overline{WRITE}$ output. The Write and Status Counters are incremented on the Low-to-High transition. $\overline{WRITE}$ output is also negated at this time, but the address bus is held in the stable state. This input is used as a control pin when presetting the internal counters and registers (see Table 1).
10	$\overline{RESET}$	I	**RESET:** A Low-to-High transition on this input resets the Read, Write and Status Counters. The address is programmed to the desired FIFO depth and the UDFLAG Register is set to reflect a Half-Full condition. MUX/LATCHs are also cleared. A Low on this pin will 3-State the address bus. $\overline{CE}$ has to be Low in order to perform any of the above functions. This input is used as a control pin when presetting the internal counters and registers (see Table 1).
9	$\overline{CE}$	I	**CHIP ENABLE:** FRC is enabled when this input is Low. When High $\overline{READ}$, $\overline{WRITE}$ and address outputs will be 3-Stated. This pin is also used as a Write input (data clocked on the Low-to-High edge) when presetting the internal counters and registers (see Table 1).
8	$\overline{BT}$	I	**BURST TRANSFER:** When Low it will allow either the Read or Write operation to function without having to interleave cycles with the other operation by disabling the other input. Resetting the device when this input is High will cause the FRC to operate in the normal (non-cascade) mode. Resetting when a Low level is present on this pin will initialize the device to operate in the cascade mode.
3	$\overline{READ}$	O	**READ:** This output goes Low after a Read request is selected to be serviced. It returns to the High state when the Read Request is removed. This pin is 3-Stated if either $\overline{CE}$ is High or $\overline{RESET}$ is Low.
4	$\overline{WRITE}$	O	**WRITE:** This output goes Low after a Write Request is selected to be serviced. It returns to the High state when the Write Request is removed. This pin is 3-Stated if either $\overline{CE}$ is High or $\overline{RESET}$ is Low.
11	FULL	I/O	**FULL:** This open-collector output becomes active-High when the used bits (adjusted for address length) of the Status Register are all ones. After a FULL condition is reached, any additional Writes will cause the FRC to scroll the memory (Read and Write Counters will increment together). A Read will always remove the FULL condition causing this output to go Low. If this pin is forced Low after a FULL condition is reached, the device will operate normally (no scrolling). The next Write after the pin is forced Low will remove the FULL condition and this output will remain Low until all of the Status Counter bits are ones again.

PIN DESCRIPTION (Continued)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
12	EMPTY	I/O	**EMPTY:** This open-collector output becomes active-High when the used bits of the Status Register are all zeroes. After an EMPTY condition is reached, any additional Reads will cause the FRC to scroll the memory. A Write will always remove the EMPTY condition causing this output to go Low. If this pin is forced Low after an EMPTY condition is reached, the device will operate normally (no scrolling). The next Read after the pin is forced Low will remove the EMPTY condition and this output will remain Low until all of the Status Counter bits are zeroes again.
13	UDFLAG	O	**UDFLAG:** If not predefined by the user, this open-collector output will become active-High when the most significant bit (adjusted for address length) of the Status Register is High and all other bits are zero (i.e. reflecting a Half-Full condition). If predefined, it will go High when the value of the Status Register is equal to the defined value (see Initialization/programming mode).
14-21 23-26	A0/PLD0 to A11/PLD11	I/O	**ADDRESS/PRELOAD DATA:** active-High data input and address output pins. When used as address outputs, they will either contain a Read or a Write address depending upon the input request. These outputs can be 3-Stated during normal operation by forcing $\overline{CE}$ High. A0 is the least significant address bit. These pins are used as active-High data inputs when programming the internal counters and registers of the device. PLD0 is the least significant preload data bit.
27	A12/PLD12 STATIN	I/O	**ADDRESS 12/** **PRELOAD DATA 12/** **STATus INput:** This pin has three different functions depending upon the mode the device is in. When used in the normal mode, this pin is an active-High output containing Bit 12 of either a Read or a Write address depending upon the input request. This output can be 3-Stated by forcing $\overline{CE}$ High. When preloading the internal counters and registers of the device, this pin becomes bit 12 of the preload data. This is an active-High input. When the device is used in the cascade mode, this pin becomes an active-High STATus INput. The status input is used to receive information for the previous device so that the Status Counter may be incremented or decremented properly. This pin should be hardwired to V_{CC} for the least significant device.
28	A13/PLD13 STATOUT	I/O	**ADDRESS13/** **PRELOAD DATA13/** **STATus OUTput:** This pin has three different functions depending upon the mode the device is in. When used in the normal mode, this pin is an active-High output containing Bit 13 of either a Read or a Write address depending upon the input request. This output can be 3-Stated by forcing $\overline{CE}$ High. When preloading the internal counters and registers of the device, this pin becomes Bit 13 of the preload data. This is an active-High input. When the device is used in the cascade mode, this pin becomes an active-High STATus OUTput. The status output is used to send information to the next device so that the Status Counter may be incremented or decremented properly.
1	A14/PLD 14/ RWIN	I/O	**ADDRESS 14/** **PRELOAD DATA 14/** **READ WRITE INput:** This pin has three different functions depending upon the mode the device is in. When used in the normal mode, this pin is an active-High output containing Bit 14 of either a Read or a Write address depending upon the input request. This output can be 3-Stated by forcing $\overline{CE}$ High. When preloading the internal counters and registers of the device, this pin becomes Bit 14 of the preload data. This is an Active-High input. When the device is used in the cascade mode, this pin becomes an active-High Read Write INput. The Read Write INput is used to receive information from the previous device so that the Read and Write counters may be incremented or decremented properly. This pin should be hard wired to V_{CC} for the least significant device.
2	A 15/PLD 15/ RWOUT	I/O	**ADDRESS 15/** **PRELOAD DATA 15/** **READ WRITE OUTput:** This pin has three different functions depending upon the mode the device is in. When used in the normal mode this pin is an active-High output containing Bit 15 of either a Read or a Write address depending upon the input request. This output can be 3-Stated by forcing $\overline{CE}$ High. When preloading the internal counters and registers of the device, this pin becomes Bit 15 of the preload data. This is an active-High input. When the device is used in the cascade mode this pin becomes an active-High Read Write OUTput. The Read Write OUTput is used to send information to the next device so that the Read and Write counters of the next device may be incremented properly.
7	V_{CC}	I	Power supply 5V ± 5%
22	GND	I	Ground

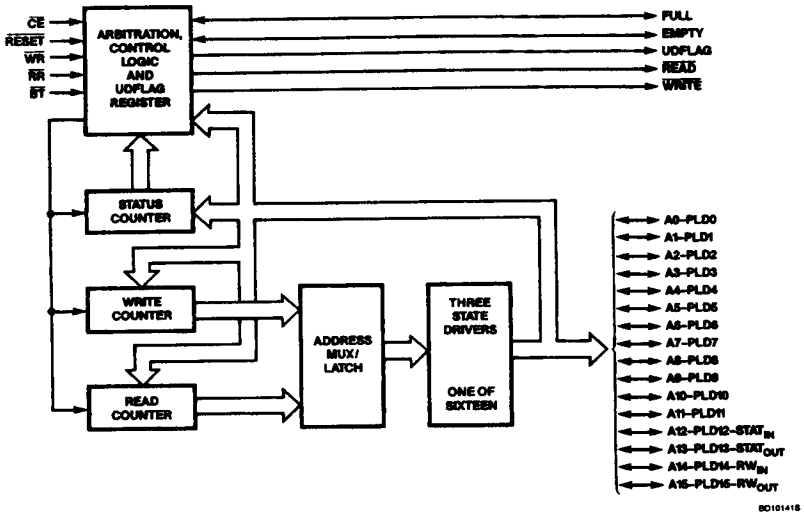


Figure 1. 74LS429 Block Diagram

Table 1. Preload/Reset Truth Table

RESET	CE	WR	RR	BT	OPERATING MODE
X	1	X	X	X	Disabled
↑	1	X	X	X	Disabled, the device will not reset
↑	0	X	X	1	Reset and operate in normal mode
↑	0	X	X	0	Reset and operate in cascade mode
0	↑	0	0	X	Preload Status Register
0	↑	0	1	X	Preload Read Counter
0	↑	1	0	X	Preload Write Counter
0	↑	1	1	X	Set UDFLAG Register

x = Don't care
0 = Low state
1 = High state
↑ = Rising edge

FUNCTIONAL OPERATION

The FRC may operate either in the normal or the cascade mode. The following description will apply to both of these modes unless otherwise specified. However, a more detailed operation in the cascade mode is included under the Cascade Mode Operation section.

The FRC operates in either of the two basic modes; Write into the FIFO buffer memory or Read from the FIFO buffer memory. However, the device may also be in the initialization (programming) or arbitration phase.

INITIALIZATION/PROGRAMMING MODE

The FRC does not wake-up in a defined state and, therefore, the user must provide a power-up reset to ensure proper operation of the device. The length of the FIFO is programmable (in multiples of 2) and is accomplished by grounding the unused address outputs through a 1K resistor. It is necessary to reset the device, each time the FIFO length is changed.

The FRC has programmable Read, Write and Status Counters. The user can initialize these counters to any desired value. When programming these counters, A0 – A15 address outputs will become inputs and should contain the pre-load data that will be written into the selected counter. The UDFLAG output of the device is also programmable and, therefore, can be set to become active at any desired time (Table 1).

Asserting a $\overline{\text{RESET}}$ after programming the above counters and UDFLAG will reset the device, i.e., Read, Write and Status Counter will be reset, UDFLAG will be set to reflect a half full condition, and address mux/latch will be cleared.

ARBITRATION MODE

Because of the asynchronous nature of the $\overline{\text{RR}}$ and $\overline{\text{WR}}$ signals, it is necessary to provide arbitration between these two to avoid the possibilities of operational conflicts. The arbitration logic in the FRC is implemented such that the $\overline{\text{WR}}$ input dominates the selection process. The $\overline{\text{RR}}$ has to occur a specified amount of time before the $\overline{\text{WR}}$ in order to be selected. If the $\overline{\text{WR}}$ occurs before the $\overline{\text{RR}}$, the $\overline{\text{WR}}$ will always be selected.

If both $\overline{\text{RR}}$ and $\overline{\text{WR}}$ occur at the same time, $\overline{\text{WR}}$ will be selected. Neither $\overline{\text{RR}}$ nor $\overline{\text{WR}}$ are latched internally.

WRITE CYCLE

To perform a write operation, $\overline{\text{WR}}$ must be Low and selected by the arbitration logic. This will cause the contents of the Write Address Counter to be output on the address bus, followed by assertion of the $\overline{\text{WRITE}}$ output. Normally, the $\overline{\text{WRITE}}$ output will be asserted after the address outputs are stable.

When the Write cycle is ended ($\overline{\text{WR}}$ is forced High), $\overline{\text{WRITE}}$ output will be negated, but the address outputs will be latched and held in the stable state until the next Read or Write Request is made.

Forcing $\overline{\text{WR}}$ High will increment both the Write and Status counters, but the Read counter will remain unchanged. The incremented value of the Write Counter will not be enabled on to the address bus until the next Write Request.

READ CYCLE

To perform a read operation $\overline{\text{RD}}$ must be Low and selected by the arbitration logic. This will cause the contents of the Read Counter to be output on the address bus, followed by assertion of the $\overline{\text{READ}}$ output. Normally, the $\overline{\text{READ}}$ output will be asserted after the address outputs are stable. When the read cycle is ended ($\overline{\text{RR}}$ is forced High), $\overline{\text{READ}}$ output will be negated, but the address outputs will be latched and held in the stable state until the next Read or a Write Request is made Forcing $\overline{\text{RR}}$ High will increment the Read Counter, decrement the Status Counter and leave the Write Counter unchanged. The incremented value of the Read Counter will not be enabled on to the address bus until the next Read Request.

CONTROL LOGIC

In addition to all the necessary internal timing, this section of the FRC is also responsible for the generation of FULL, EMPTY, UDFLAG, and the signals necessary for cascade mode operation.

CASCADE MODE INTERFACE

For applications that require more than 64K of addressing capability, two or more FRCs may be used in the cascade mode. The cascade mode circuitry is activated by resetting the device while holding the $\overline{\text{BT}}$ input Low. When the device is in the cascade mode the most significant four address outputs (A12 – A15) are used to transfer register information to the next most significant device and therefore are no longer address outputs. A0 of the next most significant device will now be A12 of the address bus and so on. It is important to distinguish between the least significant and the most significant devices. The FRC automatically makes this decision when a $\overline{\text{RESET}}$ is issued while $\overline{\text{BT}}$ is Low. The device with Pin 27 (A12/PLD12/STATIN) tied to V_{CC} is selected as the Least Significant Device (LSD) and the device with Pin 28 (A13/PLD13/STATOUT) tied to ground is selected as the Most Significant Device (MSD). In a typical configuration (see Figure 2) STATIN and RWIN of the LSD will be connected to V_{CC} and STATOUT of the MSD will be connected to ground. RWOUT of the LSD will be connected to RWIN of the next MSD, but the RWOUT of the MSD may be left floating. $\overline{\text{RESET}}$, $\overline{\text{CE}}$, $\overline{\text{BT}}$, $\overline{\text{WR}}$, and $\overline{\text{RR}}$ of all the devices will be connected to each other's corresponding inputs. Similarly FULL, EMPTY and UDFLAG outputs of all the devices will be connected to each other's corresponding outputs. The $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ outputs from either of the devices may be used to assert a read and/or a write to the memory.

CASCADE MODE OPERATION

After two or more devices have been interfaced as explained in the previous section and a $\overline{\text{RESET}}$ is issued while $\overline{\text{BT}}$ is held Low, all devices will be initialized. This will also cause the devices to distinguish themselves in their respective order in the system, i.e., least significant, next most significant and most significant. At this time STATOUT and RWOUT of all the devices connected to STATIN and RWIN of the next device will be Low.

The user may at this point desire to preload the internal registers of the devices. This can be done exactly as if a single device was being programmed (see Initialization/Programming Mode). The only distinction that has to be kept in mind this time is that PLD12 of the LSD should now be presented to PLD0 of the next most significant device and so on. When programmed for cascade mode operation, Read, Write and Status Counters of the FRC are inhibited from clocking for as long as STATIN and RWIN inputs are Low. Since STATIN and RWIN of only the LSD are High at $\overline{\text{RESET}}$, it will be the only device with Read, Write and Status Counters enabled. When the Read or Write counters of the LSD are empty or full, respectively, the next Low-to-High transition of the $\overline{\text{RR}}$ or $\overline{\text{WR}}$ will generate RWOUT. This will cause the RWIN input of the next MSD to be High, hence enabling the Read and Write counters of that device. Similarly, the STATOUT pin of the LSD will go High when the Status counter is full and a $\overline{\text{WR}}$ is made or when it is empty and a $\overline{\text{RR}}$ is made.

This will produce a High at the STATIN pin of the next MSD, hence enabling its Status Counter to increment or decrement as the case might be.

The Status flags (FULL, EMPTY and UDFLAG) will go High only when the condition they represent is true across the entire FRC array. For example the FULL flag will not go High when the LSD represents a full condition, but the next Most Significant Devices don't. This is because the Status Flag outputs of all the devices are open-collector and wired together. Therefore, any of these flag outputs will only go High when that condition holds for all the devices.

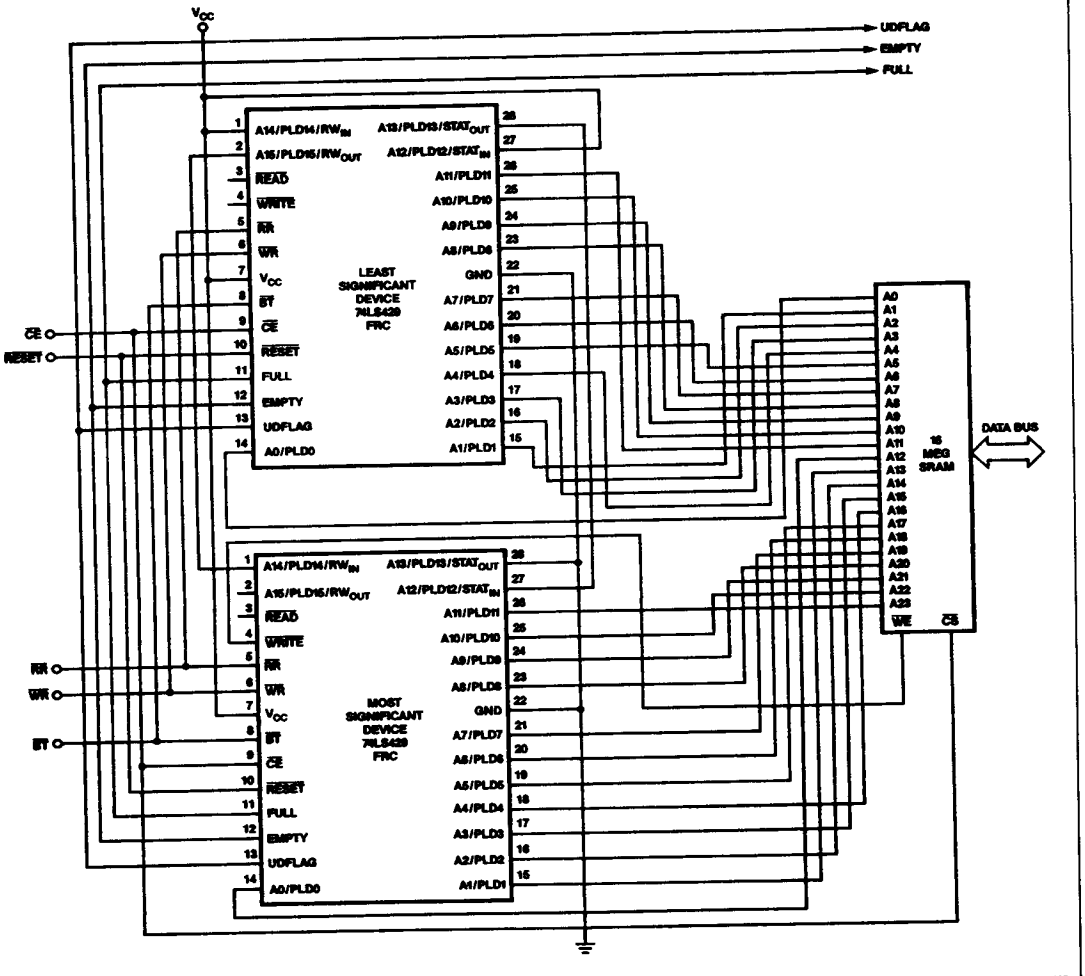


Figure 2. Cascade Mode Interface

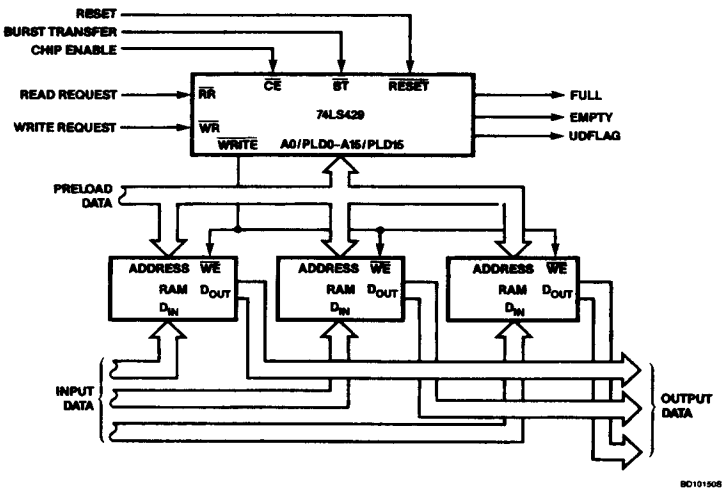


Figure 3. Converting RAMs into FIFOs Requires Simple Connections to the 74LS429 Chip. Word Lengths May be Extended by Simply Adding as Many Memory Chips in Parallel as Necessary.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1.0	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.75	5.0	5.25	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current				−3	mA
I_{OL}	Low-level output current	FULL, EMPTY, UDFLAG			8	mA
		A0 – A15, WRITE, READ			16	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		2.7			V
V_{OL}	Low-level output voltage	FULL, EMPTY UDFLAG	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 8mA			0.5	V
		READ, WRITE A0 – A15		I_{OL} = 16mA			0.5	V
V_{IK}	Input clamp voltage		V_{CC} =	$I_I = I_{IK}$			−1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				−0.4	mA
I_{OZH}	OFF-state output current High-level voltage applied		V_{CC} = MAX, V_O = 2.4V				20	µA
I_{OZL}	OFF-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				−20	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−15		−100	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				210	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = $V_{CC\ MAX}$ +0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

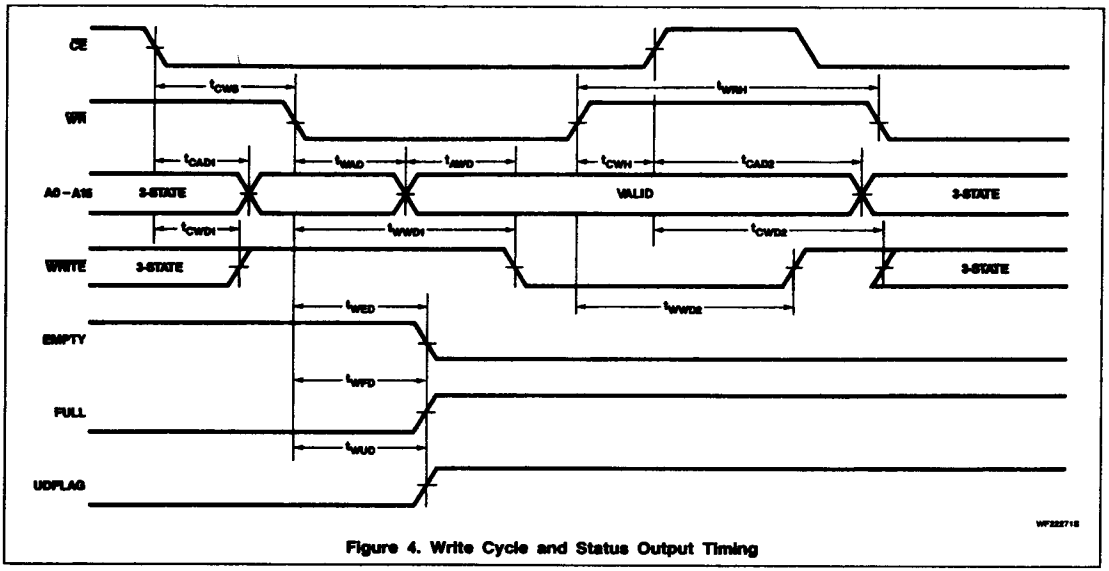


Figure 4. Write Cycle and Status Output Timing

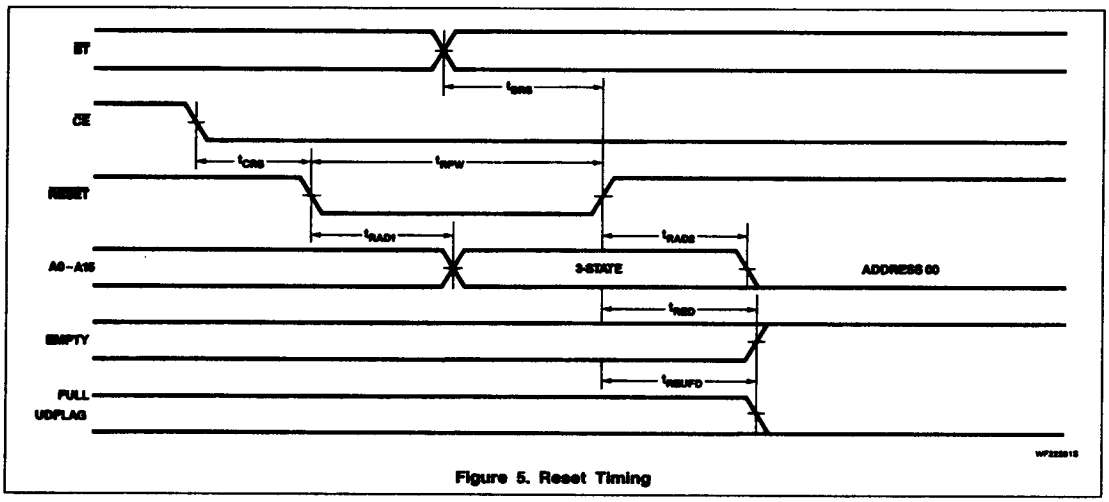


Figure 5. Reset Timing

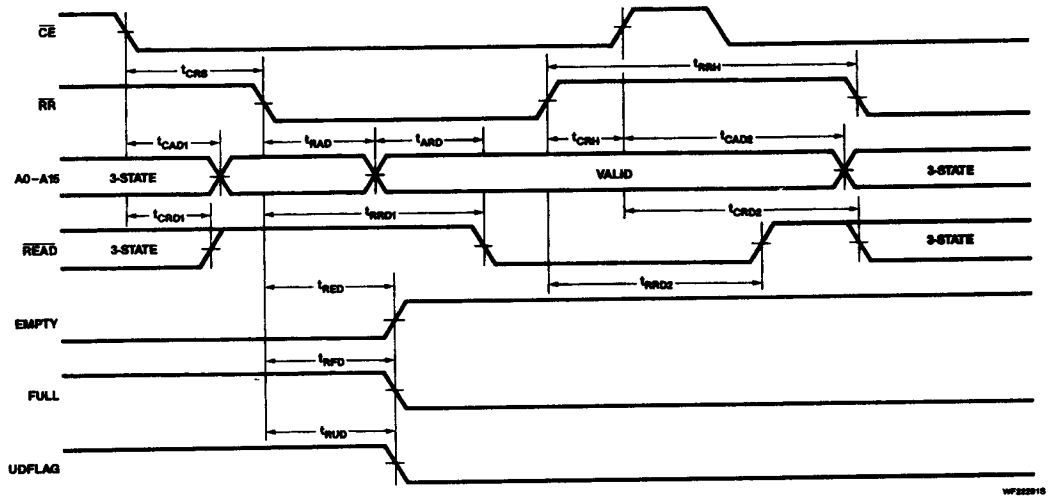


Figure 6. Read Cycle and Status Output Timing

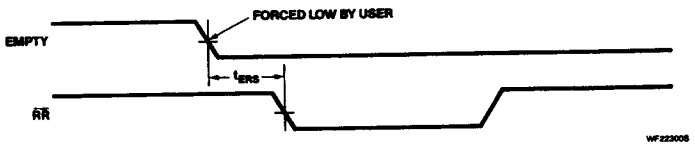


Figure 7. Empty Override Timing

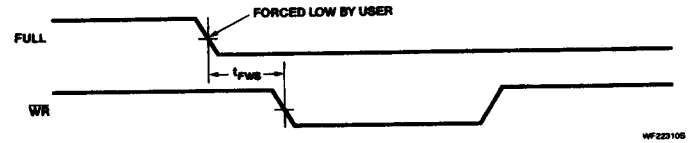


Figure 8. Full Override Timing

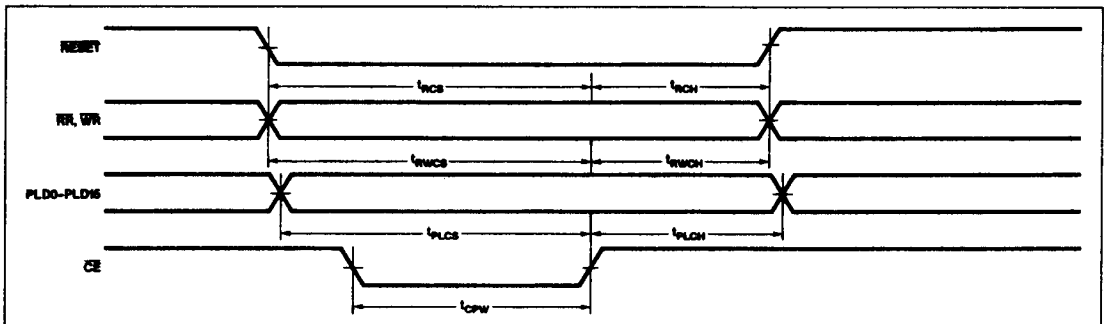


Figure 9. Pre-Load Write Cycle Timing

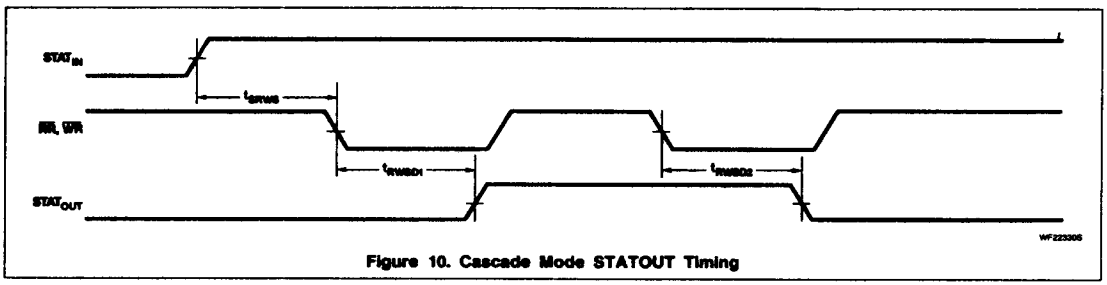


Figure 10. Cascade Mode STATOUT Timing

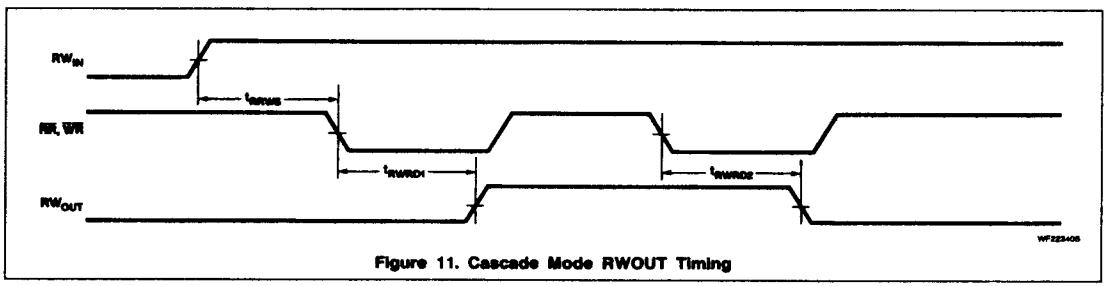


Figure 11. Cascade Mode RWOUT Timing

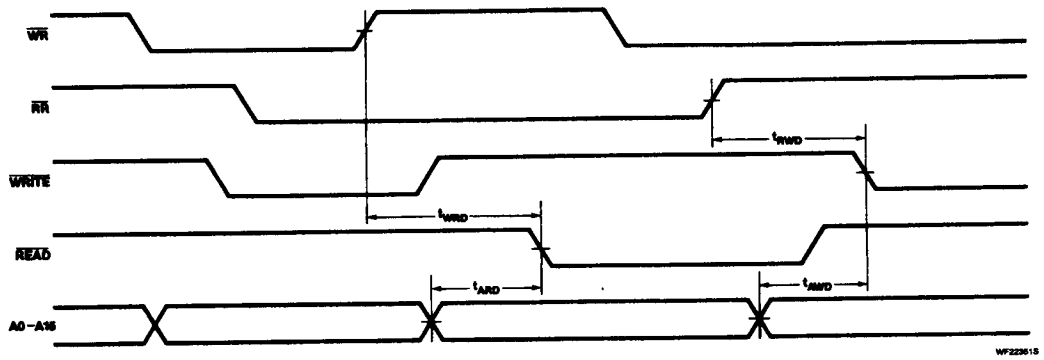


Figure 12. Change of Cycle Timing

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETERS	TEST CONDITIONS	LIMITS[1]		UNIT
			Min	Max	
Write cycle timing					
t_{CWS}	$\overline{CE}$ setup to $\overline{WR}$	AC Waveforms			ns
t_{WRH}	$\overline{WR}$ ↑ to $\overline{WR}$ ↓ hold		14		ns
t_{CWH}	$\overline{CE}$ Hold after $\overline{WR}$ ↑				ns
t_{CAD1}	$\overline{CE}$ ↓ to address delay				ns
t_{CAD2}	$\overline{CE}$ ↑ to 3-State address				ns
t_{CWD1}	$\overline{CE}$ ↓ to $\overline{WRITE}$ delay				ns
t_{CWD2}	$\overline{CE}$ ↑ to $\overline{WRITE}$ 3-State				ns
t_{WWD1}	$\overline{WR}$ ↓ to $\overline{WRITE}$ ↓ delay			26	ns
t_{WWD2}	$\overline{WR}$ ↑ to $\overline{WRITE}$ ↑ delay			11.5	ns
t_{WAD}	$\overline{WR}$ ↓ to address valid				ns
t_{AWD}	Address valid to $\overline{WRITE}$ ↓			3	ns
t_{WED}	$\overline{WR}$ ↓ to EMPTY ↓ delay				ns
t_{WFD}	$\overline{WR}$ ↓ to FULL ↑ delay				ns
t_{WUD}	$\overline{WR}$ ↓ to UDFLAG ↑ delay				ns
Read cycle timing					
t_{CRS}	$\overline{CE}$ setup to $\overline{RR}$	AC Waveforms			ns
t_{RRH}	$\overline{RR}$ ↑ to $\overline{RR}$ ↓ hold		14		ns
t_{CRH}	$\overline{CE}$ hold after $\overline{RR}$ ↑				ns
t_{CAD1}	$\overline{CE}$ ↓ to address delay				ns
t_{CAD2}	$\overline{CE}$ ↑ to 3-State address				ns
t_{CRD1}	$\overline{CE}$ ↓ to $\overline{READ}$ delay				ns
t_{CRD2}	$\overline{CE}$ ↑ to $\overline{READ}$ 3-State				ns
t_{RRD1}	$\overline{RR}$ ↓ to $\overline{READ}$ ↓ delay			26	ns
t_{RRD2}	$\overline{RR}$ ↑ to $\overline{READ}$ ↑ delay			11.5	ns
t_{RAD}	$\overline{RR}$ ↓ to address valid				ns
t_{ARD}	Address valid to $\overline{READ}$ ↓			3	ns
t_{RED}	$\overline{RR}$ ↓ to EMPTY ↑ delay				ns
t_{RFD}	$\overline{RR}$ ↓ to FULL ↓ delay				ns
t_{RUD}	$\overline{RR}$ ↓ to UDFLAG ↓ delay				ns
Override timing					
t_{ERS}	EMPTY setup to $\overline{RR}$ ↓	AC Waveforms			ns
t_{FWS}	FULL setup to $\overline{WR}$ ↓				ns

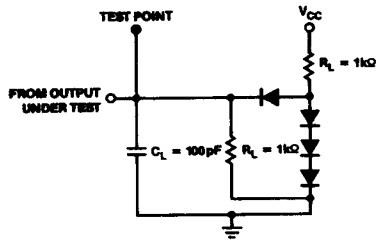
NOTE:
1. See Test Loading Circuits for loading.

AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$, $V_{CC} = 5V \pm 5\%$

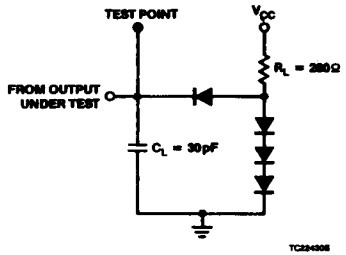
SYMBOL	PARAMETERS	TEST CONDITIONS	LIMITS[1]		UNIT
			Min	Max	
Reset timing					
t_{RPW}	RESET pulse width	AC Waveforms			ns
t_{CRS}	$\overline{CE}$ setup to $\overline{RESET}$ ↓				ns
t_{BRS}	$\overline{BT}$ setup to $\overline{RESET}$ ↑				ns
t_{RAD1}	$\overline{RESET}$ ↓ to 3-State address				ns
t_{RAD2}	$\overline{RESET}$ ↑ to all 00 address				ns
t_{RED}	$\overline{RESET}$ ↑ to EMPTY ↑				ns
t_{REUFD}	$\overline{RESET}$ ↑ to FULL ↓				ns
Pre-load data write cycle timing					
t_{CPW}	$\overline{CE}$ pulse width	AC Waveforms			ns
t_{RCS}	$\overline{RESET}$ setup to $\overline{CE}$ ↑				ns
t_{RWCS}	$\overline{RR}$, $\overline{WR}$ setup to $\overline{CE}$ ↑				ns
t_{PLCS}	PLD0 - PLD15 setup to $\overline{CE}$ ↑				ns
t_{RCH}	$\overline{RESET}$ hold after $\overline{CE}$ ↑				ns
t_{RWCH}	$\overline{RR}$, $\overline{WR}$ hold after $\overline{CE}$ ↑				ns
t_{PLCH}	PLD0-PLD15 hold after $\overline{CE}$ ↑				ns
Cascade mode timing					
t_{SRWS}	STATIN setup to $\overline{RR}$ ↓, $\overline{WR}$ ↓	AC Waveforms			ns
t_{RWSD1}	$\overline{RR}$ ↓, $\overline{WR}$ ↓ to STATOUT ↑ delay				ns
t_{RWSD2}	$\overline{RR}$ ↓, $\overline{WR}$ ↓ to STATOUT ↓ delay				ns
t_{RRWS}	RWIN setup to $\overline{RR}$ ↓, $\overline{WR}$ ↓				ns
t_{RWRD1}	$\overline{RR}$ ↓, $\overline{WR}$ ↓ to RWOUT ↑ delay				ns
t_{RWRD2}	$\overline{RR}$ ↓, $\overline{WR}$ ↓ to RWOUT ↓ delay				ns
Change of cycle timing					
t_{WRD}	$\overline{WR}$ ↑ to $\overline{READ}$ ↓	AC Waveforms			ns
t_{RWD}	$\overline{RR}$ ↑ to $\overline{WRITE}$ ↓				ns
t_{ARD}	Address valid to $\overline{READ}$ ↓			3	ns
t_{AWD}	Address valid to $\overline{WRITE}$ ↓			3	ns

NOTE:
1. See Test Loading Circuits for loading.

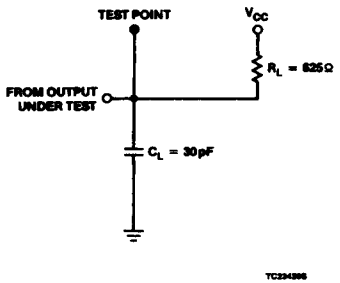
TEST LOADING CIRCUITS



Applicable Pins: All Address Outputs



Applicable Pins: (READ and WRITE)



Applicable Pins: (FULL, EMPTY and UDFLAG)

NOTES:
1. In all cases C_L includes probe and jig capacitance.
2. All diodes are 1N916, 1N3064, 1N914 or equivalent.
3. All resistors are ±1% and ¼ watt.
4. All capacitors are ±5% and 50V.