256-BIT TTL RAM (256 x 1) 54/74LS301 (O.C.)

DESCRIPTION

The 54/74LS301 is a Read/Write memory array which features an open collector output for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors, which reduce input loading.

The additional feature of output blanking during Write ($\overline{D}_O$ terminal "H") permits $\overline{D}_O$ and D_{IN} terminals to share a common I/O line to reduce system interconnections. These devices have fast Read access and Write cycle times, and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

The 54/74LS301 is available in both the commercial temperature range (0°C to +75°C) and the military temperature range (−55°C to +125°C). They are specified as: N74LS301F or N for the commercial temperature range, and S54LS301F, G, or W for the military temperature range. Military products are available as fully processed to Mil-Std 883 Level B or Level C; specify either 883B or 883C.

See page 4-9 for Truth Table, Timing Diagrams, Test Circuit and Waveform.

FEATURES

- **Address access time:**
  N74LS301: 40ns max
  S54LS301: 70ns max
- **Write cycle time:**
  N74LS301: 25ns max
  S54LS301: 60ns max
- **Power dissipation: 0.98mW/bit typ**
- **Input loading:**
  N74LS301: −100μA max
  S54LS301: −250μA max
- **Output blanking during Write**
- **On-chip address decoding**
- **Schottky clamped**
- **TTL compatible**

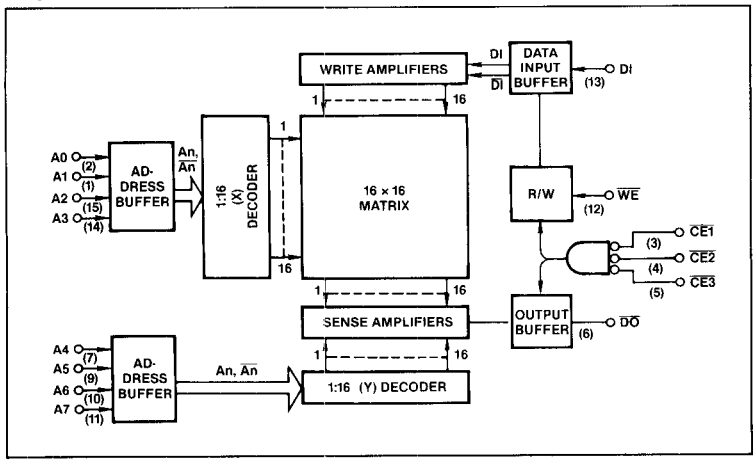
APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

ABSOLUTE MAXIMUM RATINGS

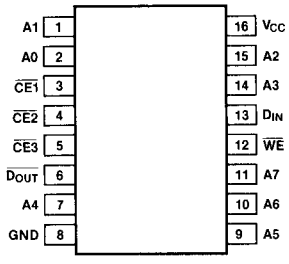
	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_{OUT}	Output voltage High (open collector)	+5.5	Vdc
T_A	Temperature Range Operating N grade S grade	 0 to +70 −55 to +125	 °C
T_{STG}	Storage	−65 to +150	°C

BLOCK DIAGRAM



PIN CONFIGURATIONS

F, N, W PACKAGE

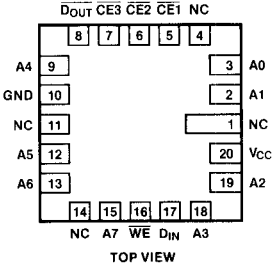


TOP VIEW

Order Numbers:

F = Cerdip N74LS301F or N74LS301N
N = Plastic S54LS301F or S54LS301W
W = Flat Pak

G PACKAGE



TOP VIEW

Order Number:
S54LS301G

G = Leadless

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DC ELECTRICAL CHARACTERISTICS

N74LS301: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S54LS301: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N74LS301			S54LS301			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage[2]								V
V_{IL}	Low	V_{CC} = min			0.85			0.8	
V_{IH}	High	V_{CC} = max	2.0			2.0			
V_{IC}	Clamp[3]	V_{CC} = min, I_{IN} = −18mA			−1.2			−1.2	
	Output voltage	V_{CC} = min							V
V_{OL}	Low[5]	I_{OL} = 16mA			0.45			0.50	
	Input current[2]	V_{CC} = max							
I_{IL}	Low	V_{IL} = 0.45V			−100			−250	μA
I_{IH}	High	V_{IH} = 2.7V			25			25	
	Output current								
I_{OLK}	Leakage[5]	V_{IH} = 2V, V_O = 5.5V			40			50	μA
I_{CC}	V_{CC} supply current[8]	V_{CC} = max		50	70		50	100	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

R1 = 270Ω, R2 = 1KΩ, C_L = 15pF
N74LS301: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S54LS301: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N74LS301			S54LS301			UNIT
				Min	Typ[1]	Max	Min	Typ[1]	Max	
	Access time									ns
T_{AA}	Address	Output	Address		30	40		30	70	
T_{CE}	Chip enable	Output	Chip enable		15	25		15	40	
T_{CD}	Disable time	Output	Chip enable		15	25		15	40	ns
T_{WD}	Valid time	Output	Write enable		30	40		30	55	ns
	Setup and hold time									ns
T_{WSA}	Setup time	Write enable	Address	0	−5		10	−5		
T_{WHA}	Hold time			0	−5		10	−5		
T_{WSD}	Setup time	Write enable	Data in	25	15		40	15		
T_{WHD}	Hold time			0	−5		10	−5		
T_{WSC}	Setup time	Write enable	$\overline{CE}$	0	−5		10	−5		
T_{WHC}	Hold time			0	−5		10	−5		
	Pulse width									ns
T_{WP}	Write enable[9]			25	15		40	15		

NOTES

1. All typical values are at V_{CC} = 5V, T_A = 25°C.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic low stored and V_{IL} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
5. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.

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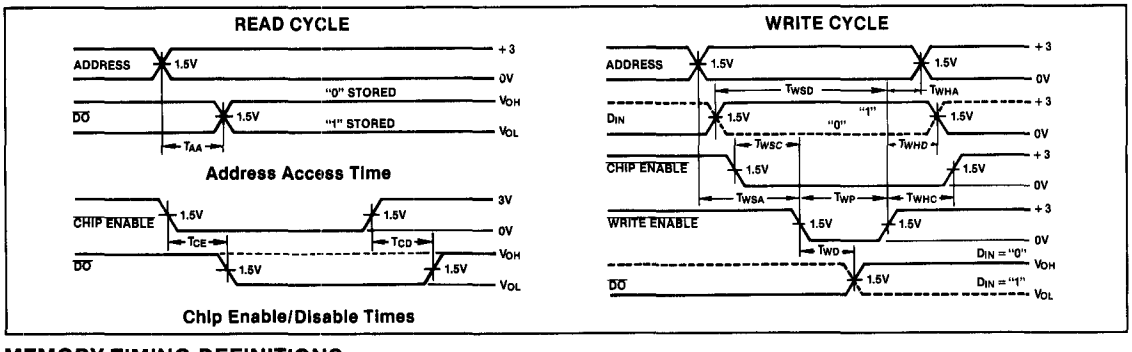
TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	D_{OUT}		
				54/74S301, 54/74LS301	82S16/LS16	82S17/LS17
Read	0	1	X	Stored data	Stored data	Stored data
Write "0"	0	0	0	1	1	1
Write "1"	0	0	1	1	0	0
Disabled	1	X	X	1	Hi-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = One or more $\overline{CE}$ inputs high.

X = Don't care.

TIMING DIAGRAMS



MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of chip enable low (with address valid) and when data output becomes valid.

T_{CD} Delay between when chip enable becomes high and data output is in off state.

T_{AA} Delay between beginning of valid address (with chip enable low) and when data output becomes valid.

T_{WSC} Required delay between beginning of valid chip enable and beginning of Write enable pulse.

T_{WHD} Required delay between end of Write enable pulse and end of valid input data.

T_{WP} Width of Write enable pulse.

T_{WSA} Required delay between beginning of valid address and beginning of Write enable pulse.

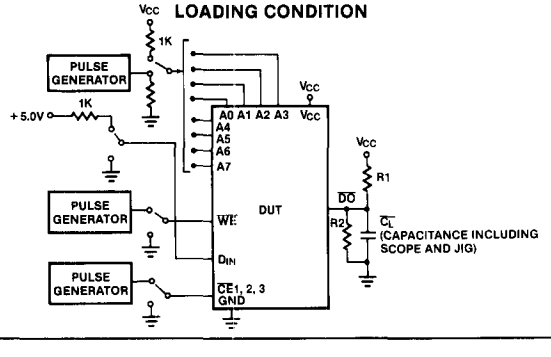
T_{WSD} Required delay between beginning of valid data input and end of Write enable pulse.

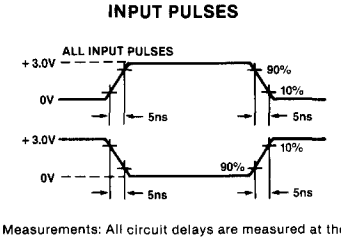
T_{WD} Delay between beginning of Write enable pulse and when data output reflects complement of data input.

T_{WHC} Required delay between end of Write enable pulse and end of chip enable.

T_{WHA} Required delay between end of Write enable pulse and end of valid address.

TEST LOAD CIRCUIT AND VOLTAGE WAVEFORM





Measurements: All circuit delays are measured at the +1.5 level of inputs and output.