

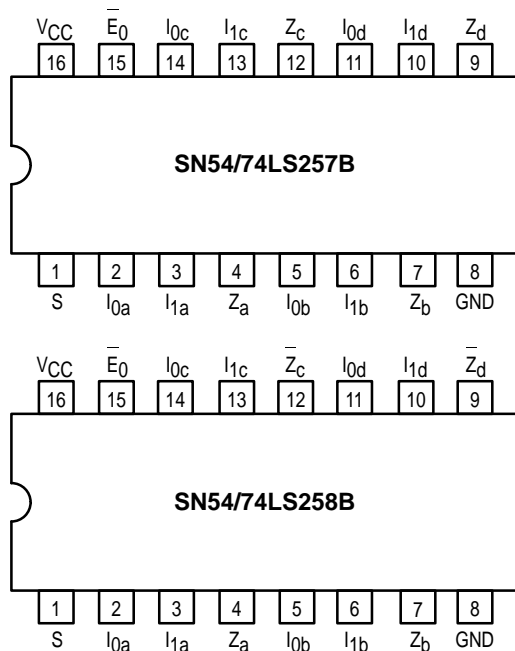


QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The LSTTL/MSI SN54/74LS257B and the SN54/74LS258B are Quad 2-Input Multiplexers with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (\bar{E}_O) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Schottky Process For High Speed
- Multiplexer Expansion By Tying Outputs Together
- Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- Special Circuitry Ensures Glitch Free Multiplexing
- ESD > 3500 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)



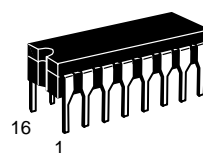
V_{CC} = PIN 16
GND = PIN 8

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

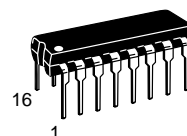
SN54/74LS257B
SN54/74LS258B

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

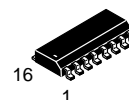
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

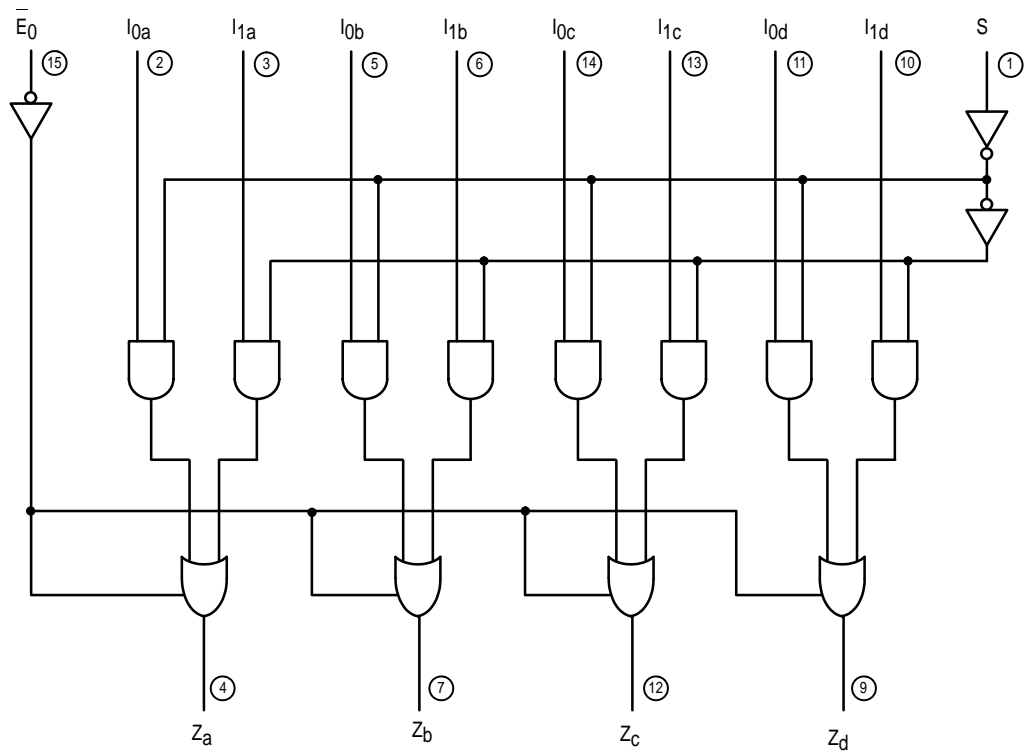
ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

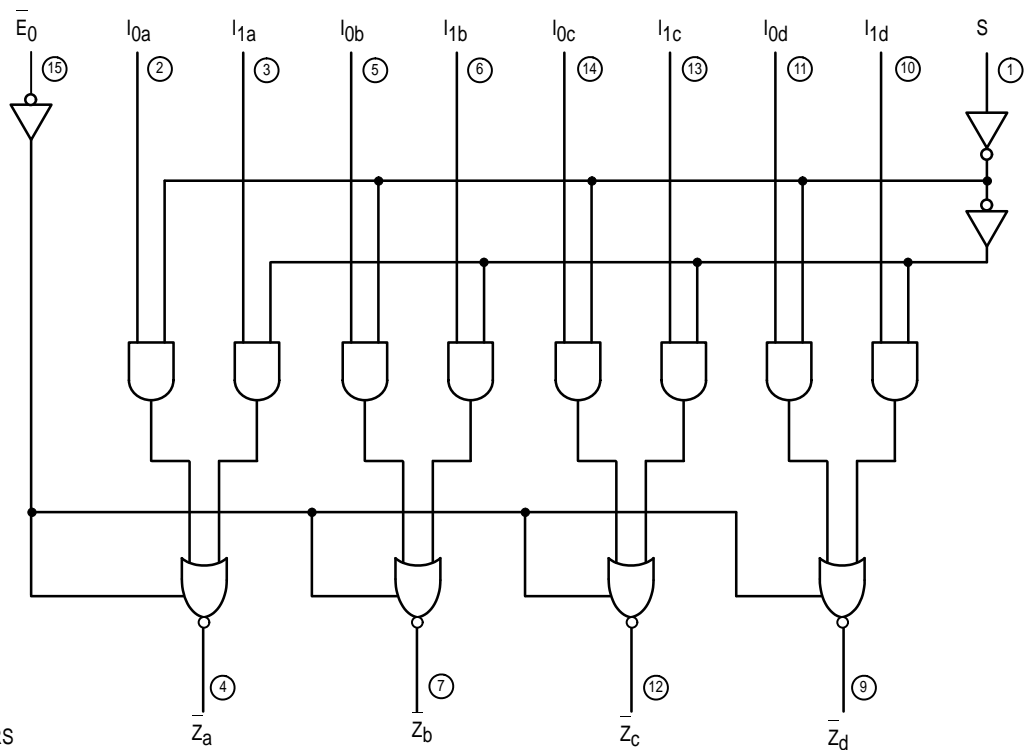
SN54/74LS257B • SN54/74LS258B

LOGIC DIAGRAMS

SN54/74LS257B



SN54/74LS258B



V_{CC} = PIN 16
 GND = PIN 8
 ○ = PIN NUMBERS

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FUNCTIONAL DESCRIPTION

The LS257B and LS258B are Quad 2-Input Multiplexers with 3-state outputs. They select four bits of data from two sources each under control of a Common Data Select Input. When the Select Input is LOW, the I₀ inputs are selected and when Select is HIGH, the I₁ inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form for the LS257B and in the inverted form for the LS258B.

The LS257B and LS258B are the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

When the Output Enable Input ($\overline{E_0}$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

LS257B

$$Z_a = \overline{E_0} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \quad Z_b = \overline{E_0} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$Z_c = E_0 \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \quad Z_d = E_0 \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

LS258B

$$Z_a = \overline{E_0} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \quad \overline{Z_b} = \overline{E_0} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$Z_c = E_0 \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \quad \overline{Z_d} = E_0 \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS LS257B	OUTPUTS LS258B
$\overline{E_0}$	S	I ₀	I ₁	Z	\overline{Z}
H	X	X	X	(Z)	(Z)
L	H	X	L	L	H
L	H	X	H	H	L
L	L	L	X	L	H
L	L	H	X	H	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 (Z) = High Impedance (off)

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54 74			-1.0 -2.6	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

SN54/74LS257B • SN54/74LS258B

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.4	3.4		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.4	3.1		V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 24 mA	
I _{OZH}	Output Off Current — HIGH				20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current — LOW				-20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current Other Inputs S Inputs				20 40	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
	Other Inputs S Inputs				0.1 0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current All Inputs				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		-30		-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH	LS257B			10	mA	V _{CC} = MAX	
		LS258B			9.0			
	Total, Output LOW	LS257B			16	mA		
	LS258B			14				
	Total, Output 3-State	LS257B			19	mA		
		LS258B			16			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V) See SN54LS251 for Waveforms

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH} t _{PHL}	Propagation Delay, Data to Output			10 12	13 15	ns	Figures 1 & 2	C _L = 45 pF
t _{PLH} t _{PHL}	Propagation Delay, Select to Output			14 14	21 21			
t _{PZH}	Output Enable Time to HIGH Level			20	25	ns	Figures 4 & 5	C _L = 45 pF R _L = 667 Ω
t _{PZL}	Output Enable Time to LOW Level			20	25			
t _{PLZ}	Output Disable Time to LOW Level			16	25	ns	Figures 3 & 5	C _L = 5.0 pF R _L = 667 Ω
t _{PHZ}	Output Disable Time from HIGH Level			18	25			