CMOS General Purpose Timer

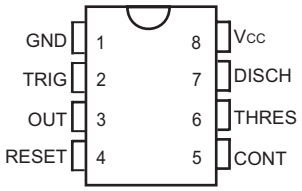
DESCRIPTION

The TLC555 is a highly stable controller capable of producing accurate timing pulses. With a monostable operation, the time delay is controlled by one external resistor and one capacitor. With an astable operation, the frequency and duty cycle are accurately controlled by two external resistors and one capacitor.

This CMOS RC timers improved parameters include low supply current, wide operating supply voltage range, low THRES, TRIG and RESET currents, no crow barring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONT for stable operation.

PIN CONFIGURATION

D,P PACKAGE



(Top View)

FEATURES

- Exact equivalent in most cases for SE/NE555
- Low supply current
- High speed operation is 500 kHz guaranteed
- Wide operation supply voltage range is 2 to 18 volts
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- High output source/sink driver can drive TTL/CMOS

APPLICATION

- Precision Timing
- Pulse Generation
- Time Delay Generation
- Sequential Timing
- Pulse width modulation
- Missing Pulse Detector

ORDERING INFORMATION

Temperature Range	Package		Orderable Device	Package Qty
-40°C to +85°C	DIP-8L	Pb-Free	TLC555P	50Units/Tube
	SOP-8L		TLC555D	100Units/Tube

SCHEMATIC DIAGRAM

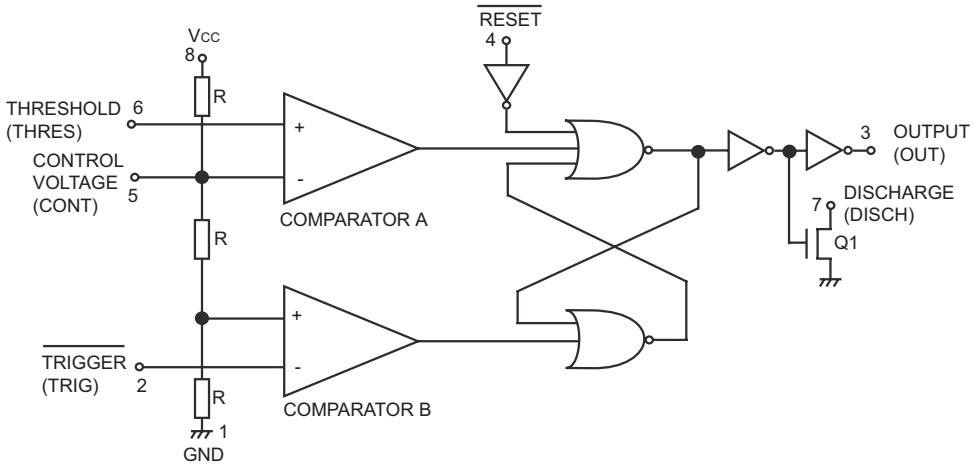


Figure 1. Block Diagram

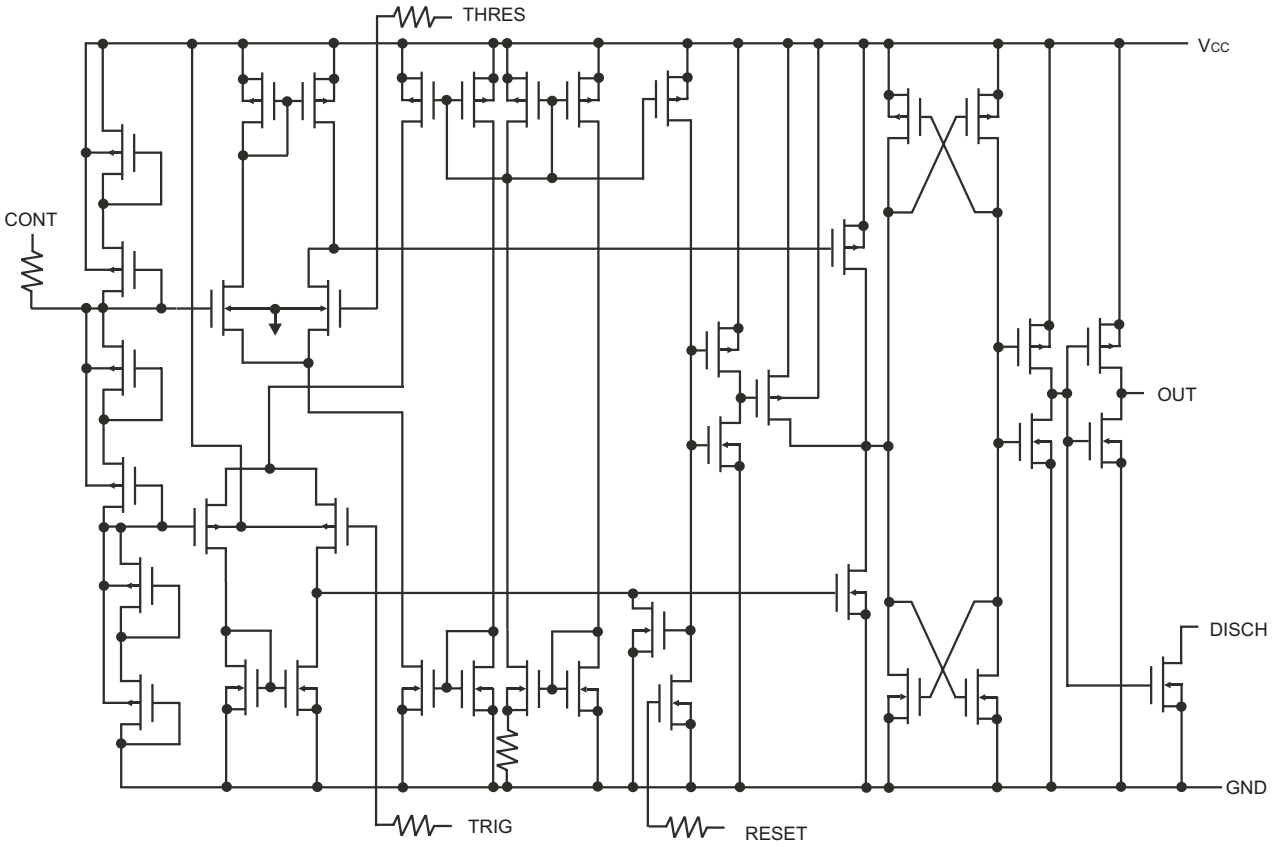


Figure 2. Cricuit Schematic

TRUTH TABLE

THRES	TRIG	RESET	OUT	DISCH
X	X	L	L	ON
> Vcc *2/3	> Vcc *1/3	H	L	ON
< Vcc *2/3	> Vcc *1/3	H	STABLE	STABLE
X	< Vcc *1/3	H	H	OFF

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	0 to 18	V
Output Current	I_O	100	mA
THRES Voltage	V_{TH}	-0.3 to V_{CC} +0.3	V
TRIG Voltage	V_{TRIG}	-0.3 to V_{CC} +0.3	V
RESET Voltage	V_{RST}	-0.3 to V_{CC} +0.3	V
Power Dissipation	P_D	200	mW
Storage Temperature	T_{STG}	-65 to +150	°C
Lead Temperature, 1mm from Case for 10 Seconds	T_L	260	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	2	18	V
Output Current	I_O		20	mA
Operating Temperature	T_A	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Threshold Voltage	V_{TH}	V_{CC} =5V	T_A =25±10°C	0.65 V_{CC}		0.70 V_{CC}	V
			T_A =-40 to +85°C	0.65 V_{CC}		0.70 V_{CC}	
Trigger Voltage	V_{TRIG}	V_{CC} =5V	T_A =25±10°C	0.31 V_{CC}		0.36 V_{CC}	
			T_A =-40 to +85°C	0.28 V_{CC}		0.40 V_{CC}	
Reset Voltage	V_{RST}	V_{CC} =2 to 18V	T_A =25±10°C	0.4 V_{CC}		1.0 V_{CC}	
			T_A =-40 to +85°C	0.2 V_{CC}		1.5 V_{CC}	
Control Voltage Lead	V_{CV}	T_A =25±10°C		0.65 V_{CC}		0.69 V_{CC}	
		T_A =-40 to +85°C		0.60 V_{CC}		0.80 V_{CC}	
Output Voltage Low	V_{OL}	T_A =25±10°C	V_{CC} =5V, I_{OL}=3.2mA			0.4	
			V_{CC} =15V, I_{OL}=20mA			1.0	
		T_A =-40 to +85°C	V_{CC} =5V, I_{OL}=3.2mA			0.6	
			V_{CC} =15V, I_{OL}=20mA			1.5	
Output Voltage High	V_{OH}	I_{OH} =-0.8mA	V_{CC} =5V, T_A=25±10°C	4.0			
			V_{CC} =15V, T_A=25±10°C	14.3			
			V_{CC} =5V, T_A=-40 to +85°C	3.5			
			V_{CC} =15V, T_A=-40 to +85°C	14			

DC ELECTRICAL CHARACTERISTICS(CONTINUED)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Supply Current	I_{CC}	T_A =25±10°C	V_{CC} =2V			200	µA
			V_{CC} =18V			300	
		T_A =-40 to +85°C	V_{CC} =2V			400	
			V_{CC} =18V			600	

AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Rise(Fall) Time of Output	t_{THL}, t_{TLH}	R_L=10MΩ, C_L=10pF	T_A =25±10°C	35		75	ns
			T_A =-40 to +85°C	70		150	
Guaranteed Max Osc. Freq.	f_{MAX}	Astable, V_{CC}=2~18V	T_A =25±10°C	500			kHz
			T_A =-40 to +85°C	200			
Initial Accuracy	ACCUR			5			%
Drift with Temperature	αf	R_L=1 to 100kΩ, C_L=0.1µF, T_A=0 to 70°C	V_{CC} =5V			0.02	%/°C
			V_{CC} =10V			0.03	
			V_{CC} =15V			0.06	
Drift with Supply Voltage	Δf	R_L=1 to 100kΩ, C_L=0.1µF, V_{CC}=5V	T_A =25±10°C			3	%/V
			T_A =-40 to +85°C			6	

Note 1: R_L ,C_L are defined in Figure 5.

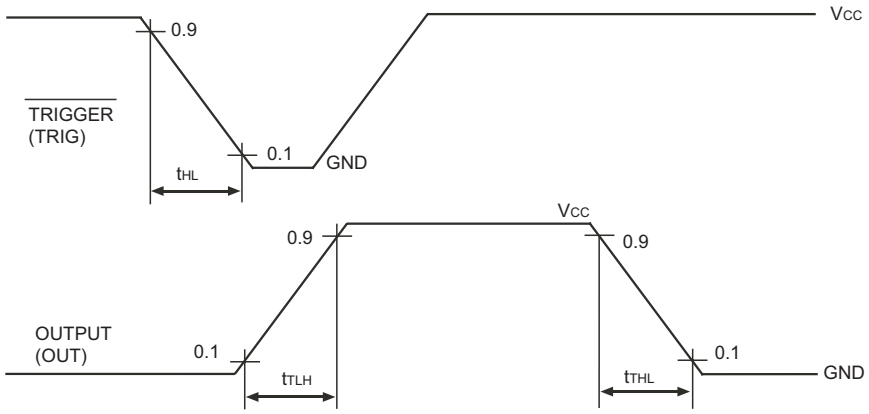


Figure 3. Swithcing Waveforms

PIN FUNCTION DESCRIPTION

No.	Name	Description
1	GND	Circuit ground pin.
2	TRIG	This trigger pin is the input to the comparator B and is used to set the latch, which in turn causes the output to go high. This is the beginning of the timing sequence in monostable operation. Triggering is accomplished by taking the pin from above to below a voltage level of 1/3 Vcc. The action of the TRIG pin is level-sensitive, allowing slow rate-of-change waveforms, as well as pulses, to be used as trigger sources.
3	OUT	The state of the output pin will always reflect the inverse of the logic state of the latch. This relationship may be best explained in terms of latch-input trigger conditions. To trigger the output to a high condition, the TRIG pin is momentarily taken from a higher to a lower level. The output can be returned to a low state by causing the THRES pin to go from a lower to a higher level, which resets the latch. The output can also be made to go low by taking the RESET pin to a low state near ground.
4	RESET	This reset pin is also used to reset the latch and return the output to a low state.
5	CONT	This control voltage pin allows direct access to the 2/3 Vcc voltage-divider point, the reference level for the comparator A. It also allows indirect access to the comparator B, as there is a 2:1 divider from this point to the comparator B reference input. Use of this terminal is the option of the user, but it does allow extreme flexibility by permitting modification of the timing period, resetting of the comparator, etc.
6	THRES	This is one input to the comparator A and is used to reset the latch, which causes the OUT pin to go low. Resetting via this terminal is accomplished by taking the terminal from below to above a voltage level of 2/3 Vcc. The action of the THRES pin is level sensitive, allowing slow rate-of-change waveforms.
7	DISCH	This pin is low resistance to ground when the OUT pin is low, and is high resistance to ground when the OUT pin is high. Usually the timing capacitor is connected between DISCH pin and ground, and is discharged when it effectively shorted to ground.
8	V_{CC}	Positive supply voltage

APPLICATION INFORMATION

Monostable Operation

For monostable operation, any of these timers can be connected as shown in Figure 4. If the output is low, application of a negative-going pulse to the TRIG sets the flip-flop, drives the output high, and turns off Q1. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the THRES input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop, drives the output low, and discharges C through Q1.

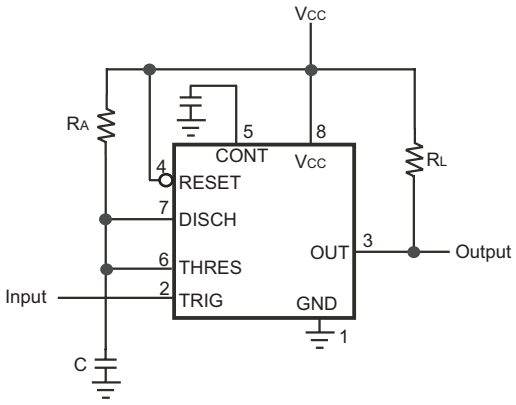


Figure 4. Cricuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high at the end of the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_W = 1.1R_AC$. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{CC}. The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to V_{CC}.

Astable Operation

As shown in Figure 5, adding a second resistor, R_B, connecting the TRIG input to the THRES input causes the timer to self-trigger and run as a multi-vibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level (≈0.67V_{CC}) and the trigger-voltage level (≈0.33V_{CC}). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.

APPLICATION INFORMATION(CONTINUED)

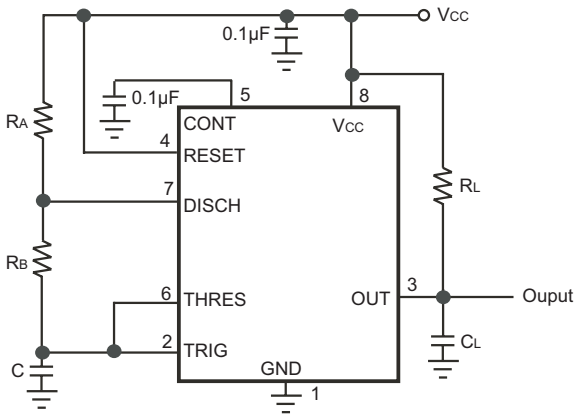


Figure 5. Cricuit for Astable Operation

The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$t_H = 0.693(R_A+R_B)C$
$t_L = 0.693R_BC$
Other useful relationships are shown below.
period = $t_H+t_L = 0.693(R_A+2R_B)C$
frequency ≈ $1.44 / ((R_A+2R_B)C)$
Output driver duty cycle = $t_L / (t_H+t_L) = R_B / (R_A+2R_B)$
Output waveform duty cycle = $t_H / (t_H+t_L) = 1 - R_B / (R_A+2R_B)$
Low-to-high ratio = $t_L / t_H = R_B / (R_A+R_B)$

Missing-Pulse Detector

The circuit shown in Figure 6 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is retriggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse.

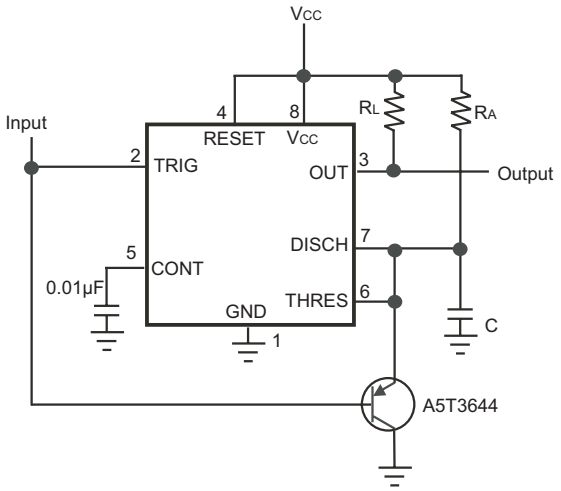


Figure 6. Cricuit for Missing-pulse Detector

APPLICATION INFORMATION(CONTINUED)

Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 7 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage.

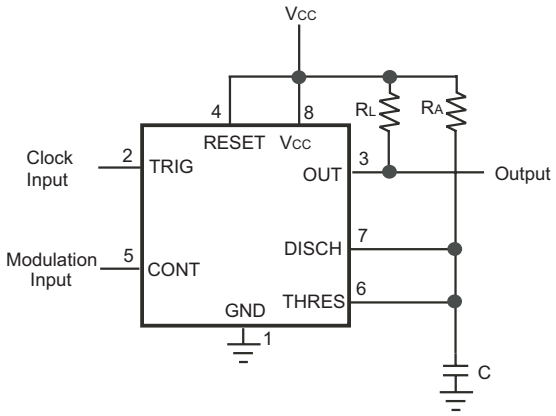


Figure 7. Cricuit for Pulse-width Modulation

Pulse-Position Modulation

As shown in Figure 8, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator.

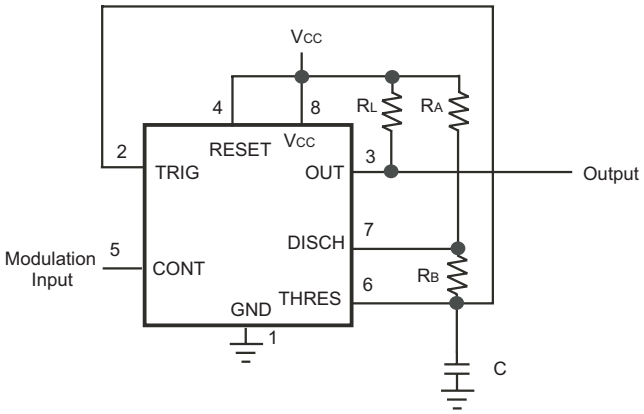
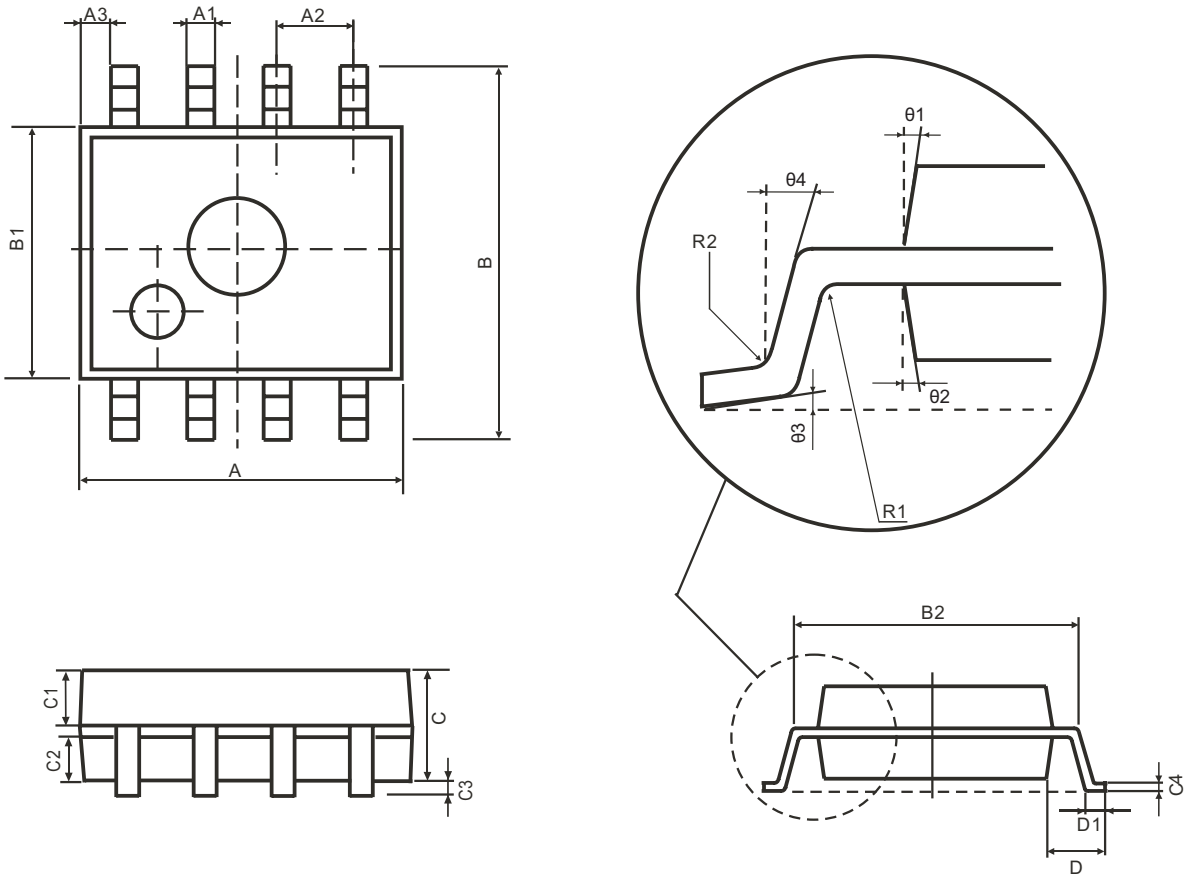


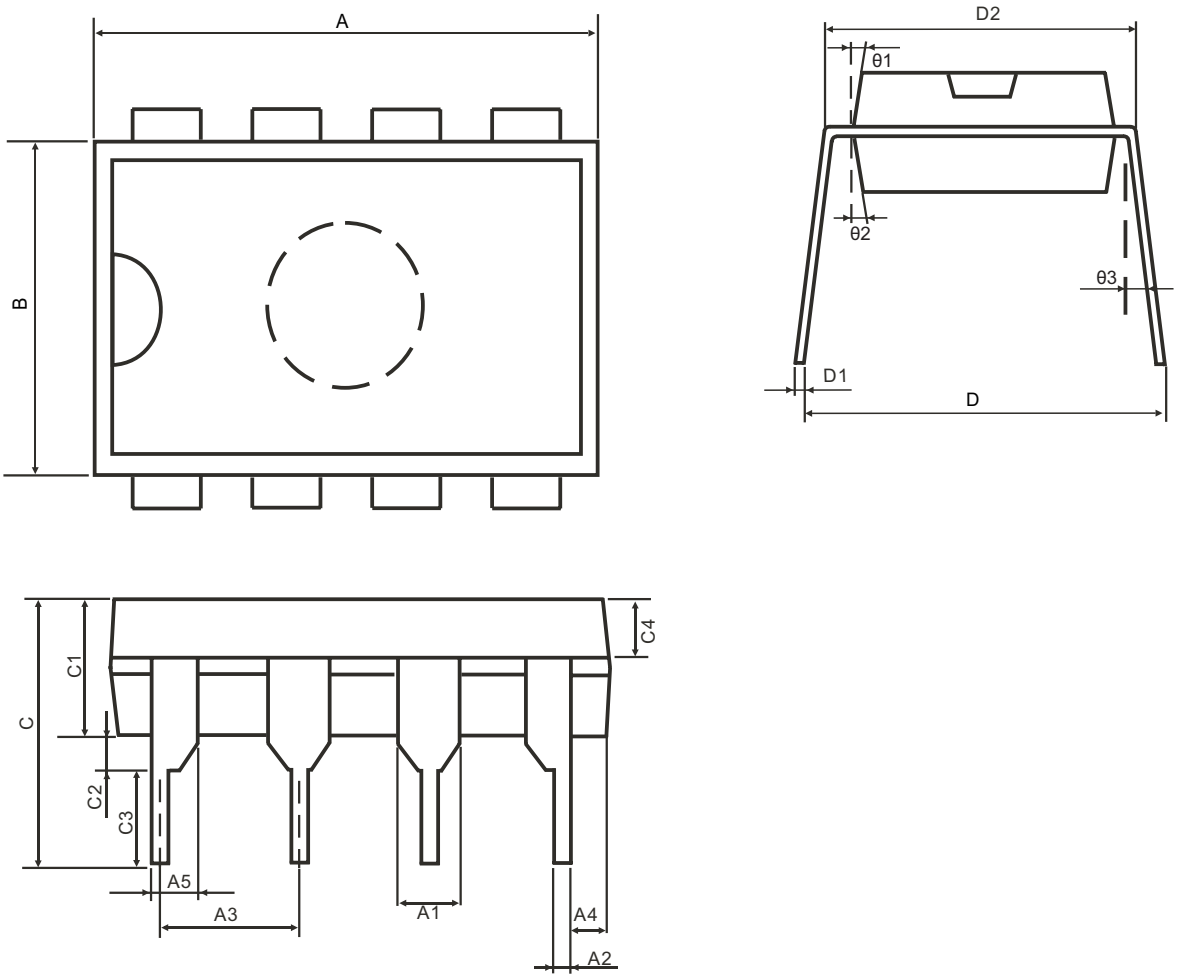
Figure 8. Cricuit for Pulse-position Modulation

PHYSICAL DIMENSIONS
SOP8L



Symbol	Dimension(mm)		Symbol	Dimension(mm)	
	Min	Max		Min	Max
A	4.95	5.15	C3	0.05	0.20
A1	0.37	0.47	C4	0.20(TYP)	
A2	1.27(TYP)		D	1.05(TYP)	
A3	0.41(TYP)		D1	0.40	0.60
B	5.80	6.20	R1	0.07(TYP)	
B1	3.80	4.00	R2	0.07(TYP)	
B2	5.0(TYP)		θ1	17°(TYP)	
C	1.30	1.50	θ2	13°(TYP)	
C1	0.55	0.65	θ3	4°(TYP)	
C2	0.55	0.65	θ4	12°(TYP)	

DIP8L



Symbol	Dimension(mm)		Symbol	Dimension(mm)	
	Min	Max		Min	Max
A	9.30	9.50	C2	0.5(TYP)	
A1	1.524(TYP)		C3	3.3(TYP)	
A2	0.39	0.53	C4	1.57(TYP)	
A3	2.54(TYP)		D	8.20	8.80
A4	0.66(TYP)		D1	0.20	0.35
A5	0.99(TYP)		D2	7.62	7.87
B	6.3	6.5	θ1	8°(TYP)	
C	7.20(TYP)		θ2	8°(TYP)	
C1	3.30	3.50	θ3	5°(TYP)	